SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**

(●) **Final Specification**

Title	55" UHD(QWUXGA) OLED

BUYER	General
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LW550AQD
SUFFIX	EMA1

APPROVED BY	SIGNATURE DATE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE DATE
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OLED TV Development Dept.
LG Display Co., Ltd.

CONTENTS

RECORD OF REVISIONS

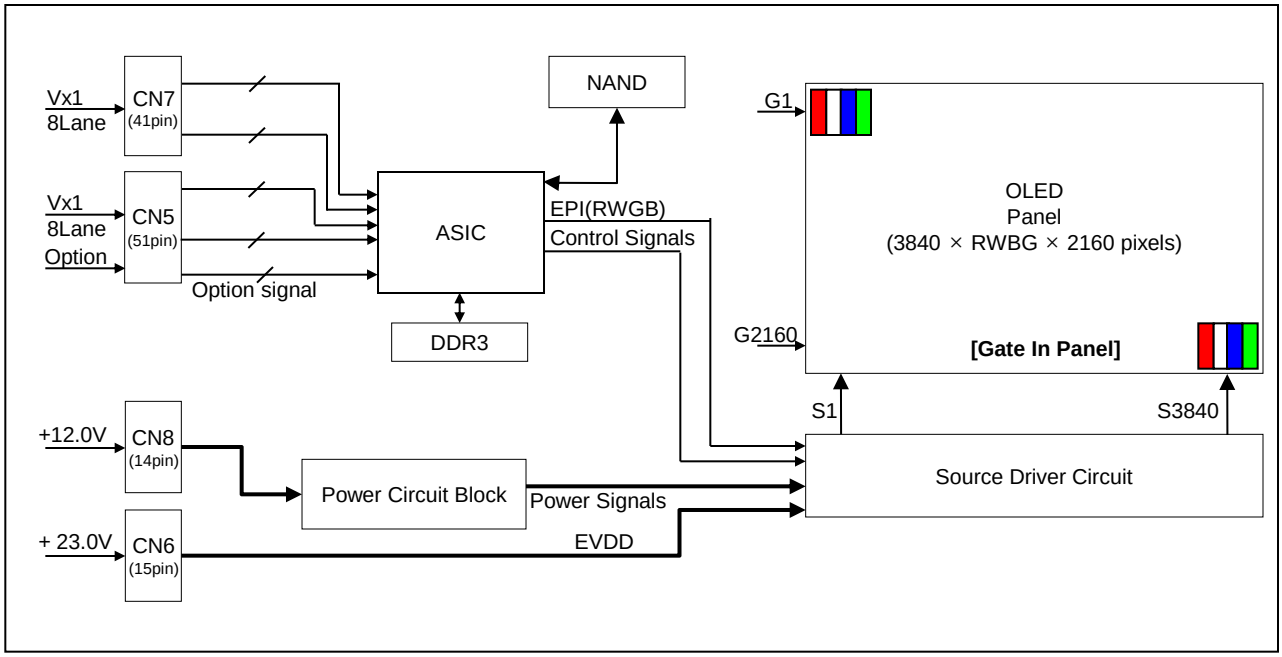
Revision No.	Revision Date	Page	Before	After	Application Date
0.0	Sep.12. 2018	-	Preliminary Specification (First Draft)		
0.1	Nov. 1. 2018	12	-	Add Timing Table for VRR mode	
0.2	Dec. 12 2018	44, 45	-	G to G and MPRT Updated	
		7	min(20.0v),Typ (21.0v),Max (22.1v)	min(20.9v),Typ (22.0v),Max (23.2v)	
			- TBD TBD - TBD TBD - TBD TBD - TBD TBD - TBD TBD - TBD TBD - TBD TBD - TBD TBD	- 1.70(TBD) 2.04(TBD) - 2.33(TBD) 2.68(TBD) - 1.73(TBD) 2.08(TBD) - 8.85(TBD) 9.74(TBD) - 20.4TBD) 24.5(TBD) - 26.8(TBD) 32.2(TBD) - 38.1(TBD) 45.7(TBD) - 185.4(TBD) 204.0(TBD)	
		8, 9	Connector (CN6): GT05S-51S-H38(LSM) or FI-RE51S-HF(JAE) Connector (CN7) : GT05S-41S-H38(LSM) or FI-RE41S-HF(JAE)	Connector(CN5):FI-RE51S-HF(JAE) or IS050-C51B-C39-C (UJU) Connector(CN7):FI-RE41S-HF(JAE) or IS050-C41B-C39-C (UJU)	
		11	-	Note. 4. Delete	
		12	2) It would not work usually under still image & reliability test. Under those condition,	2) under still image & reliability test. Under those condition,	
			“Can’t be guaranted”	Delete “Can’t be guaranted”	
		17	T3 : 0.5s	T3 : 0.54s	
			I2C is able to be accessed from **700ms** after VDD 90% rising.	I2C is able to be accessed from **540ms** after VDD 90% rising.	
		20	Gx(0.260) / Gy(0.677)	Gx(0.265) / Gy(0.682)	
			Surface Luminance, white Normal /150, Peak / 500	Changed Normal /130, Peak / 300	
			-	MPRT Delete (@ CMO ON)	
		26	-	Added “FFC Tape“	
		29	-	Added "The result should be no panel crack”	
0.3	Mar. 14 2019	1	-	Changed Buyer and Model Name	
		5	-	Changed Outline Dimension	
0.4	Apr. 02 2019	20	-	DCI → CIE1976	
		21	-	Add Note. 9. (Gamma Measurement Method)	

RECORD OF REVISIONS

Revision No.	Revision Date	Page	Before	After	Application Date
0.5	May. 10 2019	21	Surface Luminance, white Normal 130, Peak 300	Changed Normal 130, Peak 300, HDR3% 400	
		22	Gamma Measurement Method @ 25% Box	Changed @ 3% Box for 2.2 Gamma with HDR	
		6	Weight 14.5Kg(typ.)	Weight 12.5Kg(typ.)	
		28	Include Shock/Vibration	Delete Shock/Vibration	
		33	Pallet Label for LGE	Pallet Label for Non LGE	
		26	-	Drawing update	
0.6	Jun. 4 2019	21	-	Note 2. Measurement Method Change	
		20	-	Added “sRGB” Spec.	
		28	Enviroments	Changed ROHS Commission Delegated	
0.7	Jul.10 2019	29	Information of OLED Module Label 13 digits	Change Information of OLED Module Label 14 digits(add date)	
		32	Present label format	Change Label format	
		21	-	Adding Note 10.	
		26	-	Drawing update	
1.0	Jul.12 2019	18	T1 min 270sec / max 300sec T4 min 310sec	T1 min 140ses / max 170sec T4 min 180sec	
		12	-	DCLK Min/Max key in Horizontal Min/Max key in Vertical Min/Max key in	
				Final Release	

1. General Description

The **LW550AQD** is a Color Active Matrix Organic Light Emitting Diode Display (OLED).
The matrix employs Oxide Thin Film Transistor as the active element. It is a Bottom emission display type.
It has 55 inch diagonally measured active display area with QWUXGA resolution (2160 vertical by 3840 horizontal pixel array).
Each pixel is divided into Red, Green, Blue and White sub-pixels or dots which are arrayed in vertical stripes.
Gray scale or the luminance of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.
Therefore, it can present a palette of more than 1.07B(true) colors.
It has been designed to apply the 10-bit 16-lane V by One interface.
It is intended to support TV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	54.6” (1387.832 mm) diagonal
Outline Dimension (Typ.)	1225.9(H) x 700.2(V) x 4.6(B) mm (Typ.) (Flat Length)
Pixel Pitch	0.315 mm x 0.315 mm
Pixel Format	3840 horiz. by 2160 vert. Pixels, RWBG stripe arrangement
Color Depth	10bit(R), 1.07Billon colors
Luminance, White	300 / 130 cd/m^2 (Center 1point ,Typ.)
Color Viewing Angle	R/L 120 (min.), U/D 120 (min.) (Δu’v’ ≤ 0.025)
Power Consumption	**Total 58.5W (Typ.) [Logic = 20.4 W , EVDD = 38.1W @ IEC62087]**
Weight	12.5kg (Typ.)
Display Mode	Normally black
Surface Treatment	Hard coating(2H), Anti-reflection treatment of the front polarizer (Reflectance Typ. 1.2%)

2. Absolute Maximum Ratings

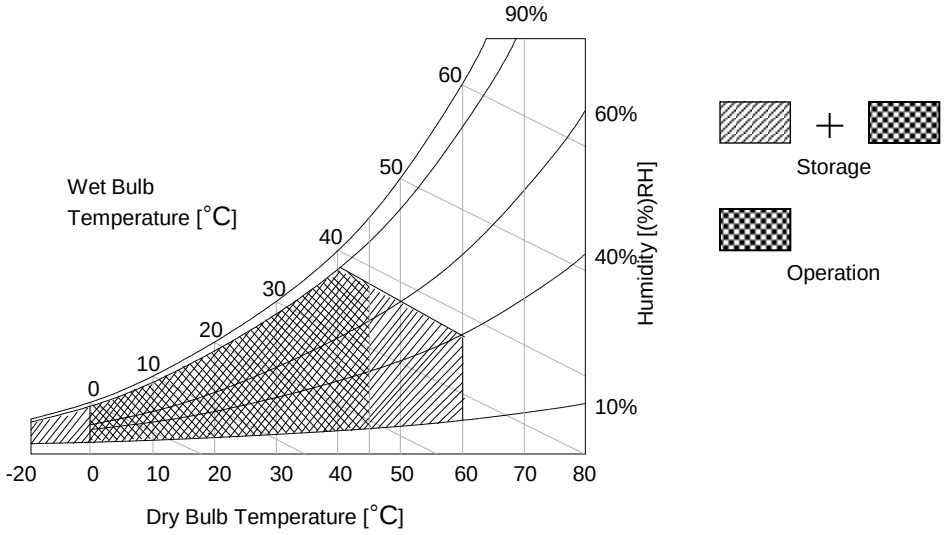
The following items are maximum values which, if exceeded, may cause faulty operation or damage to the OLED module.

Table 1. Absolute Maximum Ratings

Parameter		Symbol	Value		Unit	Note
			Min	Max		
Power Input Voltage	Logic	VDD	-0.3	+14.0	VDC	1
	EVDD	EVDD	-0.3	+ 26.0	VDC	
T-Con Option Selection Voltage		VLOGIC	-0.3	+3.7	VDC	
Operating Temperature		TOP	0	+45	°C	2
Storage Temperature		TST	-20	+60	°C	
Panel Front Temperature		TSUR	-	(+68)	°C	3
Operating Ambient Humidity		HOP	10	90	%RH	2
Storage Humidity		HST	10	90	%RH	

Note:

1. Ambient temperature condition (Ta = 25 ± 2 °C)
2. Temperature and relative humidity range are shown in the figure below.
   Wet bulb temperature should be Max 39°C, and no condensation of water.
3. The maximum operating temperatures is based on the test condition that the surface temperature of display area is less than or equal to 68°C with OLED module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68℃. The range of operating temperature may be degraded in case of improper thermal management in final product design.



3. Electrical Specifications

3-1. Electrical Characteristics

It requires two power inputs. One is employed to power for the circuit. The other is used for the EVDD.

Table 2. Electrical Characteristics

Parameter	Symbol		Values			Unit	Notes
			Min	Typ	Max		
Power Input Voltage	VDD		10.8	12.0	13.2	V	
	EVDD		20.9	22.0	23.1		
Power Input Current	I_{VDD}		-	1.70	2.04	A	1.1
			-	2.33	2.68		1.2
	I_{EVDD}		-	1.73	2.08		1.1
			-	8.85	9.74		1.3
Power Consumption	P_{VDD}		-	20.4	24.5	Watt	1.1
			-	26.8	33.6		1.2
	P_{EVDD}		-	38.1	45.7		1.1
			-	197.7	214.2		1.3
Rush current	I_{RUSH}	I_{RUSH_VDD}	-	-	7.0	A	
		I_{RUSH_EVDD}	-	-	11.3		
		T_{RUSH_VDD}	-	-	100	us	
		T_{RUSH_EVDD}	**-**	**-**	**2**	ms	

Note

1.1. The specified current and power consumption are under the VDD=12.0V, EVDD=22.0V Ta=25 ± 2°C, f_V=120Hz condition whereas standard moving picture(IEC62087) is displayed and f_V is the frame frequency.

1.2. The current (I_{VDD}) is specified at the maximum current pattern (1by1 Horizontal Pattern)

1.3. The current (I_{EVDD}) is specified at the maximum current pattern (Secondary Color Pattern).

3-2. Interface Connections

This OLED module employs two kinds of interface connection, 51-pin connector and 41-pin connector are used for the module signals and three 14-pin connectors is used for the module powers.

3-2-1. OLED Module (Signals)

- Module Connector(CN5): FI-RE51S-HF(JAE) or IS050-C51B-C39-C (UJU)
- Mating Connector : FI-RE51HL(JAE) or compatible

Table 3. Module Connector(CN5) Pin Configuration

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	NC (Reserved)	No Connection (Reserved)	27	GND	Ground
2	NC (Reserved)	No Connection (Reserved)	28	Rx0n	V-by-One HS Data Lane 0
3	NC (Reserved)	No Connection (Reserved)	29	Rx0p	V-by-One HS Data Lane 0
4	NC (Reserved)	No Connection (Reserved)	30	GND	Ground
5	NC (Reserved)	No Connection (Reserved)	31	Rx1n	V-by-One HS Data Lane 1
6	NC (Reserved)	No Connection (Reserved)	32	Rx1p	V-by-One HS Data Lane 1
7	NC (Reserved)	No Connection (Reserved)	33	GND	Ground
8	NC (Reserved)	No Connection (Reserved)	34	Rx2n	V-by-One HS Data Lane 2
9	NC (Reserved)	No Connection (Reserved)	35	Rx2p	V-by-One HS Data Lane 2
10	JB&Off-RS done	JB&Off-RS done (H), Set ← Module	36	GND	Ground
11	ELVDD ON	ELVDD ON (H= On), Set → Module	37	Rx3n	V-by-One HS Data Lane 3
12	Error Detection	H=Error, L=Normal (note 4)	38	Rx3p	V-by-One HS Data Lane 3
13	I2C-SDA1	I2C for Customer	39	GND	Ground
14	I2C-SCL1		40	Rx4n	V-by-One HS Data Lane 4
15	Data Format 1	Data Format[1:0] 00:1-div, 01:2-div, 10:4-div, 11:8-div	41	Rx4p	V-by-One HS Data Lane 4
16	Data Format 0		42	GND	Ground
17	3D_EN	No Use	43	Rx5n	V-by-One HS Data Lane 5
18	I2C-SDA	I2C for Customer	44	Rx5p	V-by-One HS Data Lane 5
19	I2C-SCL		45	GND	Ground
20	EVDD Det	EVDD reset, Set ← Module	46	Rx6n	V-by-One HS Data Lane 6
21	NC	Bit Selection (10bit only)	47	Rx6p	V-by-One HS Data Lane 6
22	GND	AGP0 (note 7)	48	GND	Ground
23	GND	AGP1 (note 7)	49	Rx7n	V-by-One HS Data Lane 7
24	GND	Ground	50	Rx7p	V-by-One HS Data Lane 7
25	HTPDN	Hot plug detect	51	GND	Ground
26	LOCKN	Lock detect	-	-	-

Notes :

1. All GND (ground) pins should be connected together.
2. All Input levels of V-by-One signals are based on the V-by-One HS Standard.
3. Specific pin No. **#10** is used for compensation when power turn off.
4. Specific pin No. **#12** is used for “Power Error detection” of the OLED module.
5. Specific pins No. **#15** and **#16** are Vx1 Input Format. This module can support 1~8 division mode (Please see the Appendix VI for more information.)
6. Specific pins No. **#18** and **#19** are used only for LGD. (Do not connect)
7. Specific pins No. **#22** and **#23** are used for “No signal detection” of system signal interface. It should be GND for NSB (No Signal Black) while the system interface signal is not. If this pin is “H”, OLED module displays AGP (Auto Generation Pattern).

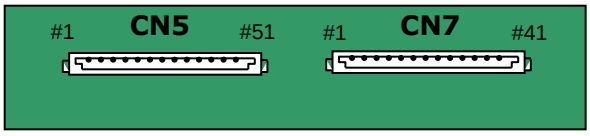
- Module Connector (CN7) : FI-RE41S-HF(JAE) or IS050-C41B-C39-C (UJU)
- Mating Connector : FI-RE41HL(JAE)or compatible

Table 4. Module Connector(CN7) Pin Configuration

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	22	GND	Ground
2	Rx8n	V-by-One HS Data Lane 8	23	Rx15n	V-by-One HS Data Lane 15
3	Rx8p	V-by-One HS Data Lane 8	24	Rx15p	V-by-One HS Data Lane 15
4	GND	Ground	25	GND	Ground
5	Rx9n	V-by-One HS Data Lane 9	26	NC	No Connection
6	Rx9p	V-by-One HS Data Lane 9	27	NC	No Connection
7	GND	Ground	28	NC	No Connection
8	Rx10n	V-by-One HS Data Lane 10	29	NC	No Connection
9	Rx10p	V-by-One HS Data Lane 10	30	NC	No Connection
10	GND	Ground	31	NC	No Connection
11	Rx11n	V-by-One HS Data Lane 11	32	NC	No Connection
12	Rx11p	V-by-One HS Data Lane 11	33	NC	No Connection
13	GND	Ground	34	NC	No Connection
14	Rx12n	V-by-One HS Data Lane 12	35	NC	No Connection
15	Rx12p	V-by-One HS Data Lane 12	36	NC	No Connection
16	GND	Ground	37	NC	No Connection
17	Rx13n	V-by-One HS Data Lane 13	38	Vx1 Byte mode	Vx1 4/5Byte mode(H:5byte, L or NC:4byte)
18	Rx13p	V-by-One HS Data Lane 13	39	QSMEN	QSMEN (Set→Module)
19	GND	Ground	40	ON_RF	ON_RF_DONE (Set ← Module)
20	Rx14n	V-by-One HS Data Lane 14	41	FW_GPIO	Firmware update Enable (Set → Module)
21	Rx14p	V-by-One HS Data Lane 14	-		

Notes : 1. All GND (ground) pins should be connected together.
2. #26~#37 NC (No Connection) : These pins are used only for LGD (Do not connect)
3. Specific pin NO.#41 is used for updating ASIC firmware, EEPROM and NAND data
It should be only “H” when set updates data.

◆ **Rear view of OLED Module**



< Top view of PCB >

3-2-2. OLED Module (Powers)

- EVDD Connector(CN6): 20022WR-H15B2(manufactured by Yeon Ho)
- Mating Connector : 20022HS-15B2(BK)(manufactured by Yeon Ho)

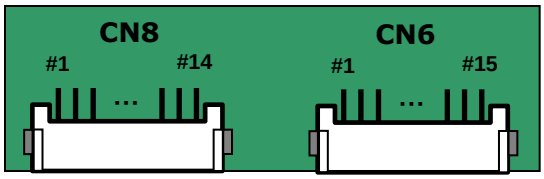
- VDD Connector(CN8) : 20022WR-H14B2(manufactured by Yeon Ho)
- Mating Connector : 20022HS-14B2(BK)(manufactured by Yeon Ho)

Table 5. EVDD / VDD Connector(CN6, CN8) Pin Configuration

No	Symbol	Description
1	EVSS	OLED Panel Ground
2	EVSS	OLED Panel Ground
3	EVSS	OLED Panel Ground
4	EVSS	OLED Panel Ground
5	EVSS	OLED Panel Ground
6	EVSS	OLED Panel Ground
7	EVSS	OLED Panel Ground
8	EVDD	OLED Panel Power Supply +21V
9	EVDD	OLED Panel Power Supply +21V
10	EVDD	OLED Panel Power Supply +21V
11	EVDD	OLED Panel Power Supply +21V
12	EVDD	OLED Panel Power Supply +21V
13	EVDD	OLED Panel Power Supply +21V
14	EVDD	OLED Panel Power Supply +21V
15	EVDD	OLED Panel Power Supply +21V

No	Symbol	Description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	VDD	Power Supply +12V
8	VDD	Power Supply +12V
9	VDD	Power Supply +12V
10	VDD	Power Supply +12V
11	VDD	Power Supply +12V
12	VDD	Power Supply +12V
13	EVDD	OLED Panel Power Supply +21V
14	NC	No connection

◆ **Rear view of OLED Module**



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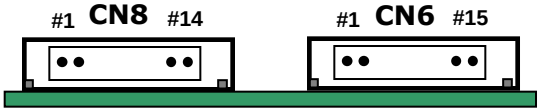


< Side view of PCB >

3-3. Signal Timing Specifications

Table 6 shows the signal timing required at the input of the V-by-One transmitter. All of the interface signal timings should be satisfied with the following specification for normal operation.

Table 6. Timing Table(DE Only Mode)

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}	240	240	240	tCLK	3840 / 16
	Blank	t_{HB}	34	35	36	tCLK	1
			0.46	0.47	0.48	us	3
	Total	t_{HP}	274	275	276	tCLK	
Vertical	Display Period	t_{VV}	2160	2160	2160	Lines	
	Blank	t_{VB}	86 (492)	90 (540)	94 (588)	Lines	1
			311 (1820)	333 (1998)	346 (2176)	us	3
	Total	t_{VP}	**2246** (2652)	2250 (2700)	2254 (2748)	Lines	

ITEM		Symbol	Min	Typ	Max	Unit	Note
Frequency	DCLK	f_{CLK}	74.00	74.25	74.50	MHz	1188 / 16
	Horizontal	f_H	268	270	272	KHz	1
	Vertical	f_V	119 (98)	120 (100)	120.5 (102)	Hz	2 NTSC (PAL)

Note: 1. The input of HSYNC & VSYNC signal does not have an effect on normal operation (DE Only Mode). If you use spread spectrum of EMI, add some additional clock to minimum value for clock margin.
2. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rate and the horizontal frequency.
3. If you change the DCLK, must satisfy the minimum horizontal & vertical blank time.

※ This OLED module supports Spread Spectrum Clocking tolerance with up to 30kHz/ ±0.5%
※ Timing should be set based on clock frequency.

Table 6-2. Timing Table(Only Gaming mode : VRR Mode)

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}	240	240	240	tCLK	3840 / 16
	Blank	t_{HB}	35	35	35	tCLK	
	Total	t_{HP}	275	275	275	tCLK	
Vertical	Display Period	t_{VV}	2160	2160	2160	Lines	
	Blank	t_{VB}	90	90	4590	Lines	
	Total	t_{VP}	2250	2250	6750	Lines	

ITEM		Symbol	Min	Typ	Max	Unit	Note
Frequency	DCLK	f_{CLK}	74.00	74.25	74.50	MHz	1188 / 16
	Horizontal	f_{H}	268	270	272	KHz	
	Vertical	f_{V}	40	120	120.5	Hz	

Note:
1. Only applicable to Gaming mode with VRR operation
2. The device could not work properly in case it is operated by VRR mode.
   1) This OLED module supports adaptive sync timing only under moving picture in room temperature(25±5℃)
   2) It would not work usually under still image & reliability test.
   3) Under those condition, the phenomenon such as image sticking, flickering, flashing and dither noise in low gray could be found on the screen.

3-4. V by One Signal Specifications

3-4-1. V by One Eye Mask Specification

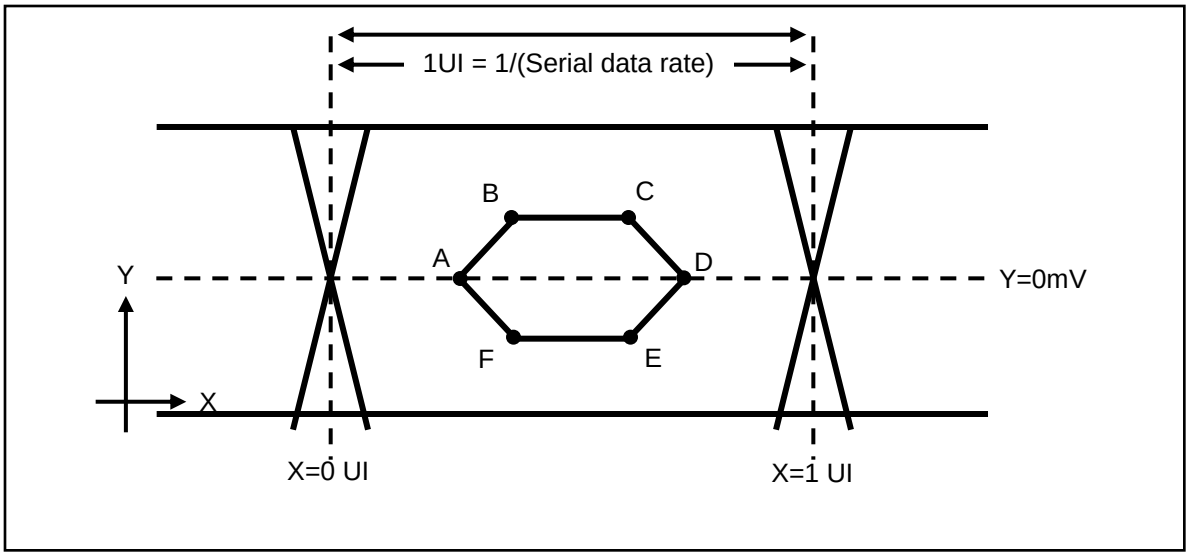


Table 7. Eye Mask Specification

	X [UI]	Note	Y [mV]	Note
A	0.25 (max)	2	0	-
B	0.30 (max)	2	50	3
C	0.70 (min)	3	50	3
D	0.75 (min)	3	0	-
E	0.70 (min)	3	|-50|	3
F	0.30 (max)	2	|-50|	3

Notes:

1.1 All Input levels of V by One signals are based on the V by One HS Standard.

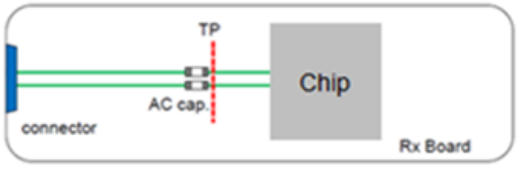
1.2 When using the Tx's Pre-Emphasis function to be set to a minimum value that meets the EYE mask spec.

2. This is allowable maximum value.

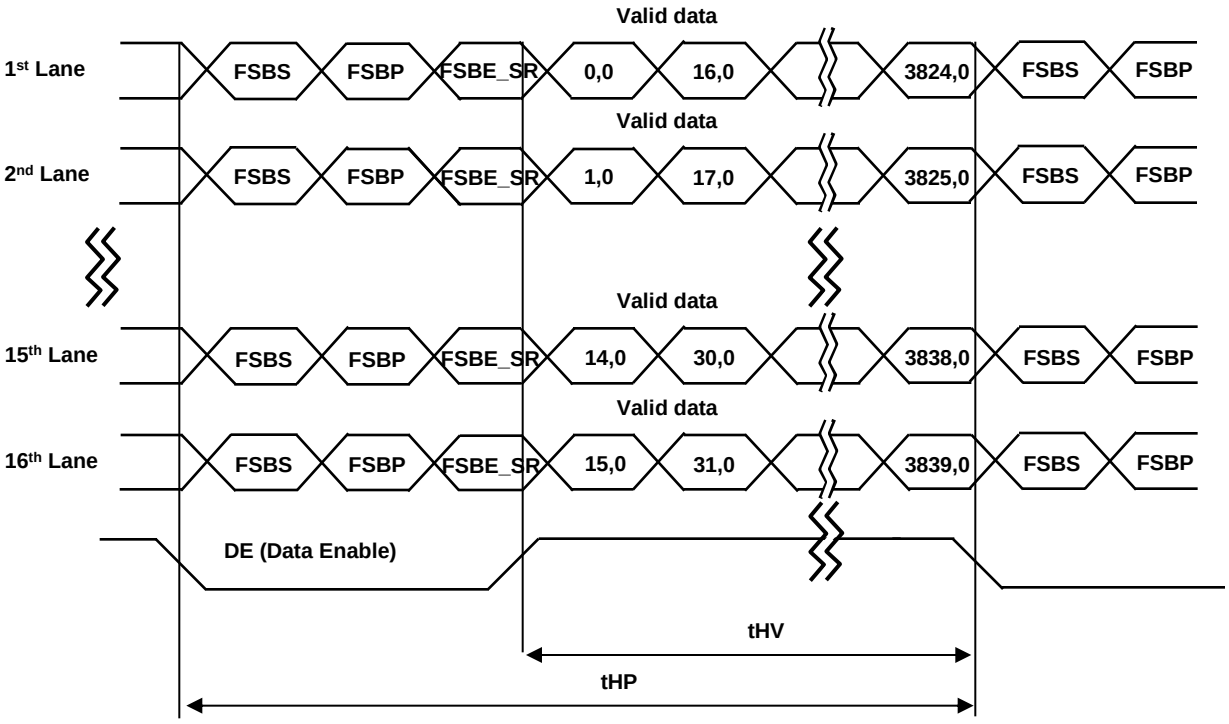
3. This is allowable minimum value.

4. The eye diagram is measured by the oscilloscope and receiver CDR characteristic must be emulated.
   - PLL type : 2nd Order
   - PLL bandwidth : 10Mhz
   - Damping Factor : 2

5. EYE mask measuring point

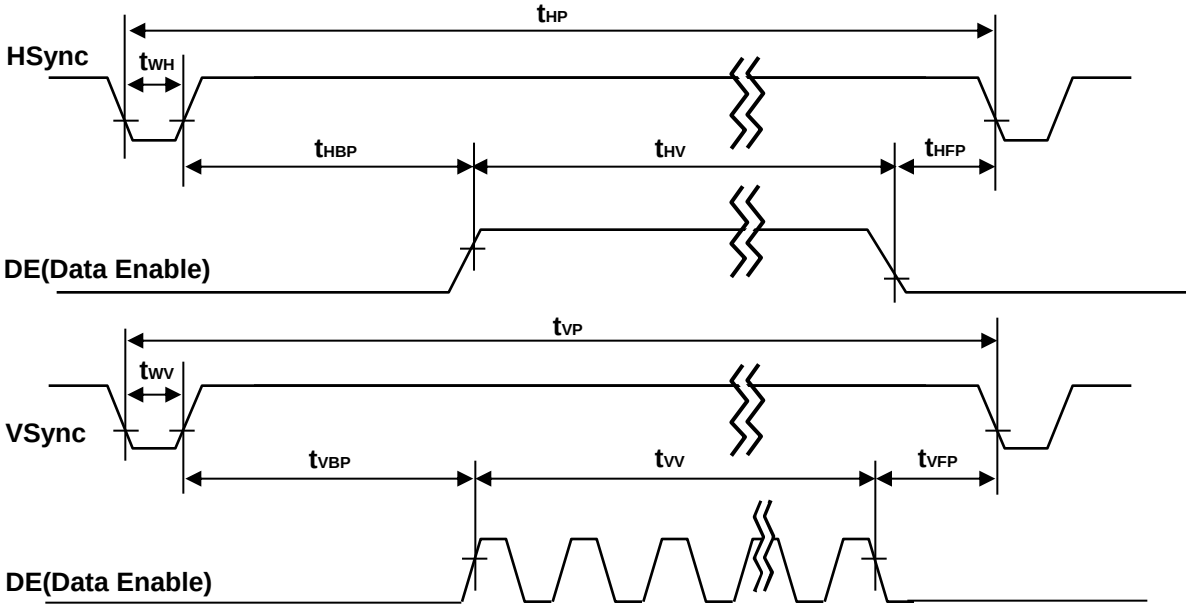


3-4-2. V by One Input Signal Timing Diagram



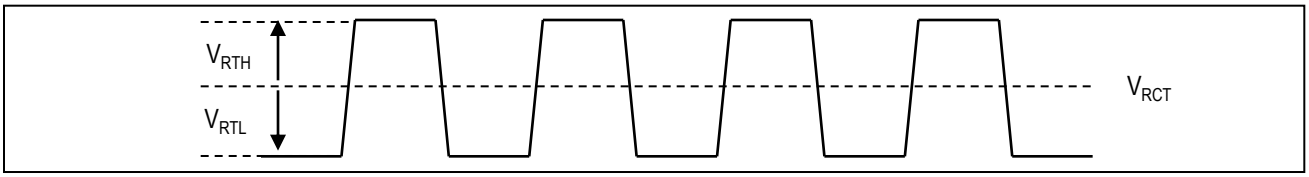
* Reference: Sync. Relation

* $t_{HB} = t_{HFP} + t_{WH} + t_{HBP}$
* $t_{VB} = t_{VFP} + t_{WV} + t_{VBP}$



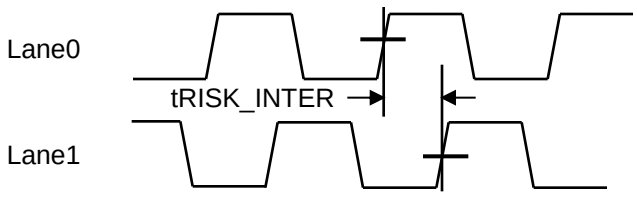
3-4-3. V by One Input Signal Characteristics

1) DC Specification

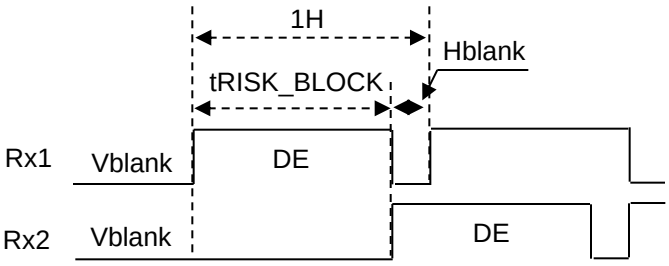


Description	Symbol	Min	Max	Unit	Note
CML Differential Input High Threshold	V_{RTH}	-	50	mV	-
CML Differential Input Low Threshold	V_{RTL}	-50	-	mV	-
CML Common Mode Bias Voltage	VRCT	0.6	0.8	V	-

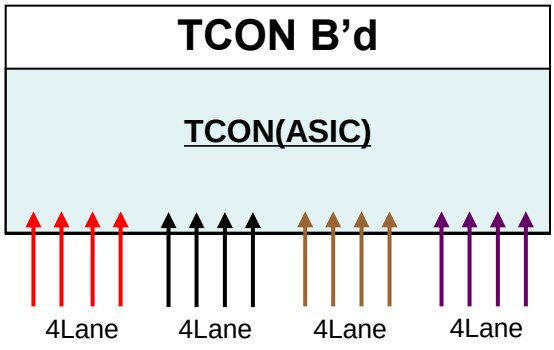
2) AC Specification



<Inter-pair skew between two lanes>



<Inter-pair skew between two sub-blocks>



<V by One Brief Diagram >

Description	Symbol	Min	Max	Unit	Note
Allowable inter-pair skew between lanes	tRISK_INTER	-	5	UI	1, 3
Allowable inter-pair skew between sub-blocks	tRISK_BLOCK	-	1	DE	1, 4

Notes: 1.1UI = 1/serial data rate

2. it is the time difference between the true and complementary single-ended signals.
3. it is the time difference of the differential voltage between any two lanes in one sub block.
4. it is the time difference of the differential voltage between any two blocks in one IP.

3-5. Color Data Reference

The brightness of each primary color (red, green, blue) is based on the 10bit or 11biy gray scale data input for the color. The higher binary input, the brighter the color. Table 8 provides a reference for color versus data Input.

Table 8. Color Data Reference

Packer input & Unpacker output		30bpp RGB (10bit)	36bpp RGB (11bit)
Byte0	D[0]	R[2]	R[4]
	D[1]	R[3]	R[5]
	D[2]	R[4]	R[6]
	D[3]	R[5]	R[7]
	D[4]	R[6]	R[8]
	D[5]	R[7]	R[9]
	D[6]	R[8]	R[10]
	D[7]	R[9]	R[11]
Byte1	D[8]	G[2]	G[4]
	D[9]	G[3]	G[5]
	D[10]	G[4]	G[6]
	D[11]	G[5]	G[7]
	D[12]	G[6]	G[8]
	D[13]	G[7]	G[9]
	D[14]	G[8]	G[10]
	D[15]	G[9]	G[11]
Byte2	D[16]	B[2]	B[4]
	D[17]	B[3]	B[5]
	D[18]	B[4]	B[6]
	D[19]	B[5]	B[7]
	D[20]	B[6]	B[8]
	D[21]	B[7]	B[9]
	D[22]	B[8]	B[10]
	D[23]	B[9]	B[11]
Byte3	D[24]	Don't care	Don't care
	D[25]	Don't care	Don't care
	D[26]	B[0]	B[2]
	D[27]	B[1]	B[3]
	D[28]	G[0]	G[2]
	D[29]	G[1]	G[3]
	D[30]	R[0]	R[2]
	D[31]	R[1]	R[3]
Byte4	D[24]	-	-
	D[25]	-	-
	D[26]	-	B[0]
	D[27]	-	B[1]
	D[28]	-	G[0]
	D[29]	-	G[1]
	D[30]	-	R[0]
	D[31]	-	R[1]

Notes 1. 30bpp RGB (10bit) is 4 byte mode , 36bpp RGB(11bit) is 5 byte mode

3-6. Power Sequence

3-6-1. OLED Driving Circuit

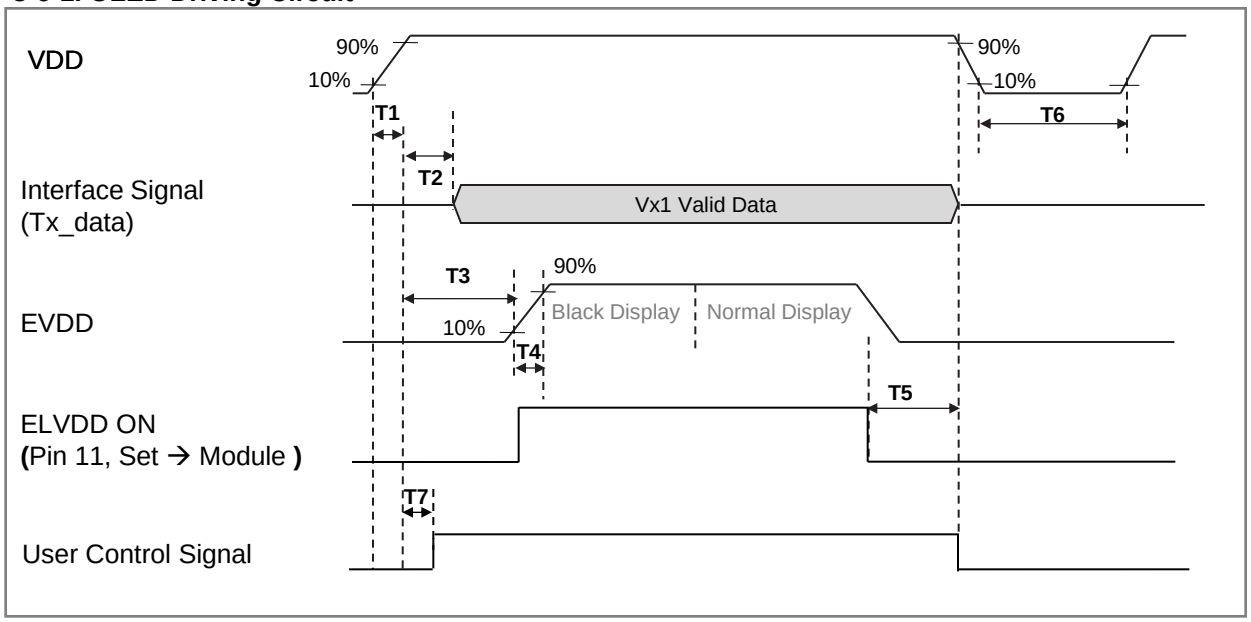


Table 9. Power Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	1	-	35	ms	1
T2	58	-	-	ms	
T3	0.54	-	-	sec	2
T4	5	-	50	ms	
T5	30	-	-	ms	
T6	1.5	-	-	sec	3
T7	0	-	T2	ms	4

Note : 1. The T3 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem. T3 should be larger than T2.

2. T6 should be measured after the module has been fully discharge between power off and on period.

3. If the on time of signals (Interface signal and user control signals) precedes the on time of Power(VDD) it will be happened abnormal display. When T7 is NC status, T7 doesn't need to be measured

4. I2C is able to be accessed from 540ms (after VDD 90% rising).

※ Black pattern is displayed during black display period before normal display. (ON RF Time 2.7s)

※ When the power for logic (VDD) turns on , EVDD should be less than 5V.
But, it does not matter if there is no garbage image.

3-6-2. OFF RS Compensation Operation

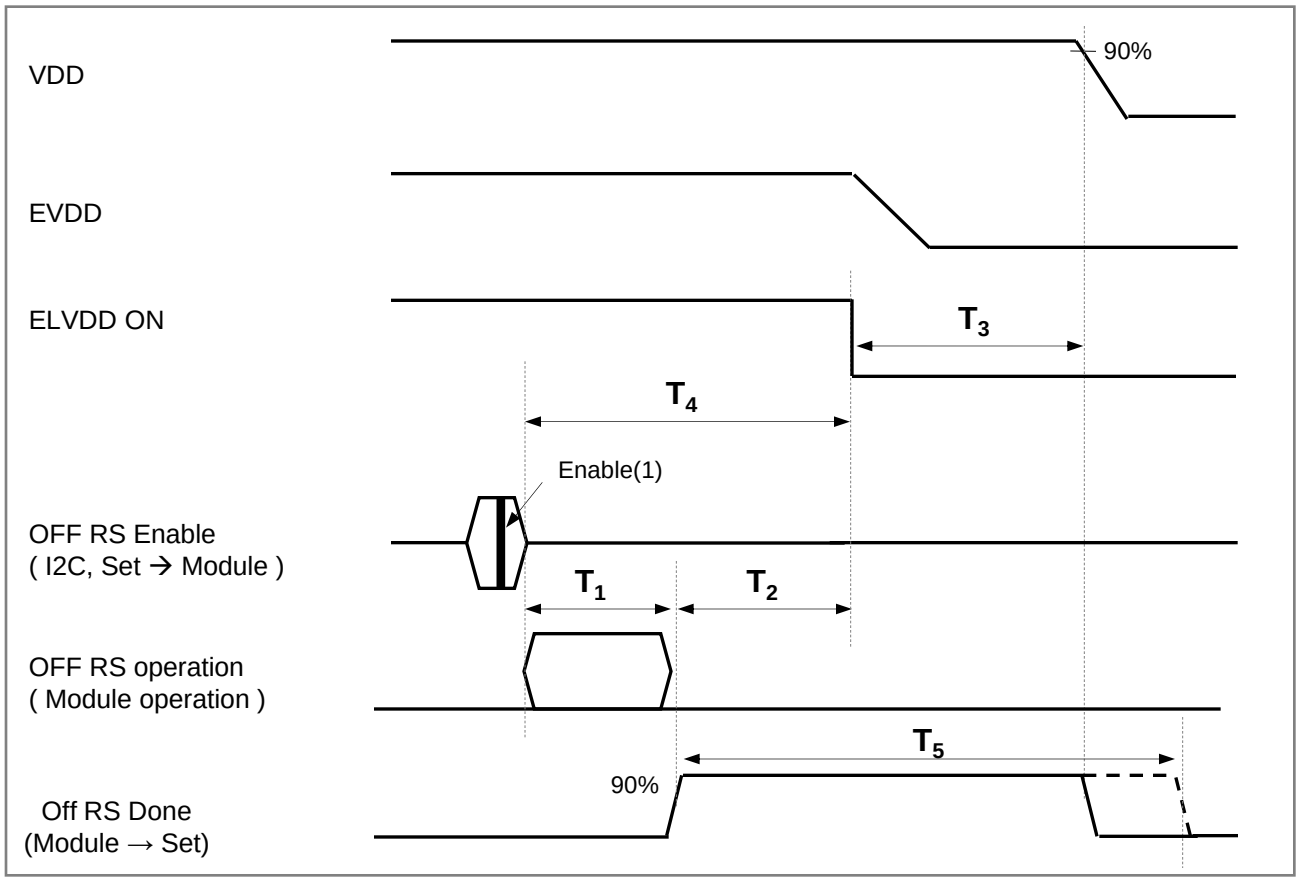


Table 10.Off-RS Power Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	140	-	170	sec	
T2	0	-	10	sec	
T3	30	-	-	ms	
T4	180	-	-	sec	
T5	0.5	7	10	sec	

Note : 1. TV system is recommended to be turned off **immediately** after T4 **min.** although Off-RS Done signal is not transferred.

※ When there is power on action before completing OFF RS operation, don't change OFF RS enable signal(1→0). Just do power off and power on.

3-6-3. JB compensation operation

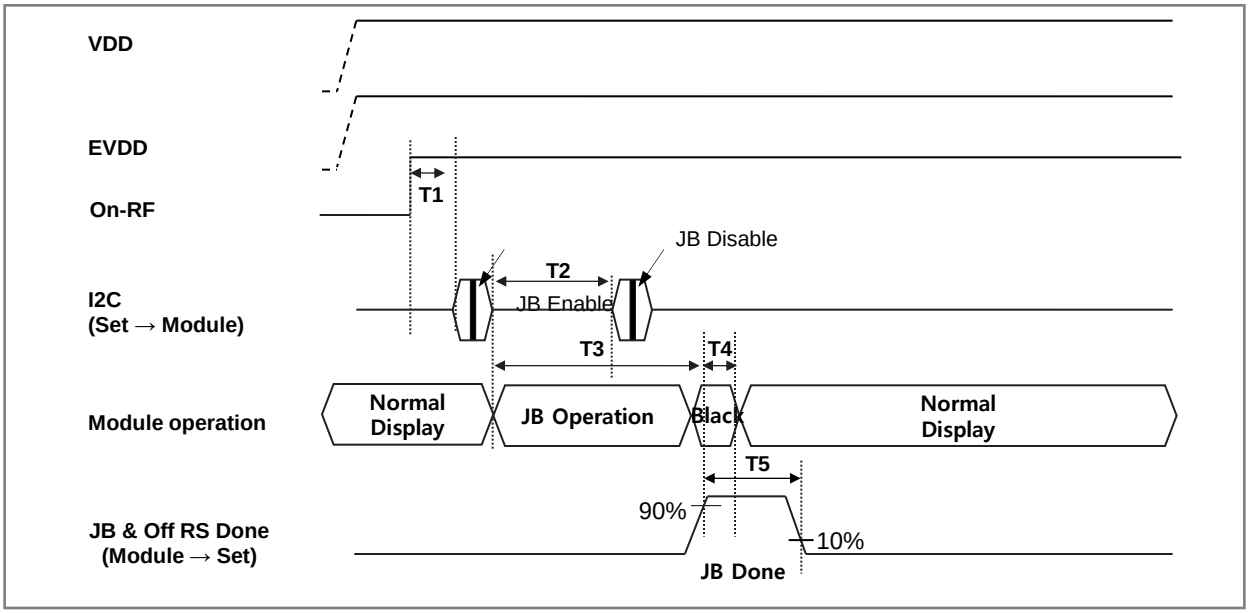


Table 11. JB Power Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	200	-	-	ms	
T2	10	-	20	sec	
T3	30	-	120	sec	
T4	110	-	130	ms	Black PTN
T5	0.5	7	10	sec	

Note : ※ JB Compensation is to be operated in conjunction with the OFFRS and it must be operated in the temperature range of JB operation, 10 to 40℃

※ JB compensation needs to be cooled during at least 1 hour more before it is operated and at this time, the TV System needs to be at the standby mode.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at distance 50cm from the OLED surface at a viewing angle of Φ and θ equal to 0 °. FIG. 1 shows additional information concerning the measurement equipment and method.

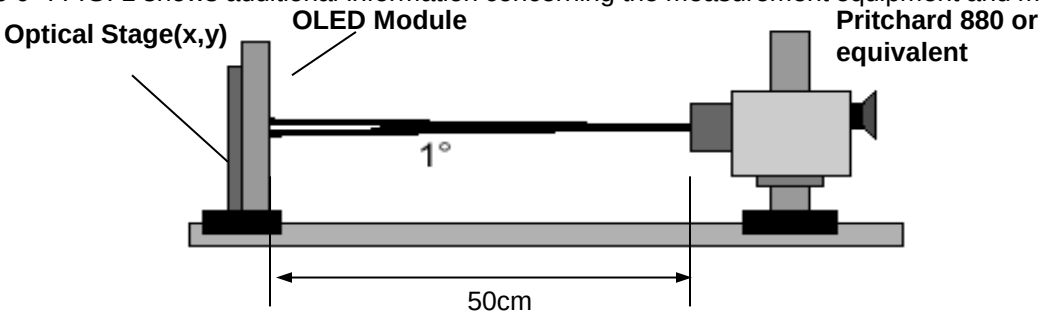


FIG. 1 Optical Characteristic Measurement Equipment and Method

Table 12. Optical Characteristics Ta= 25±2°C, VDD=12V, EVDD=21.0V, fv=120Hz, Dclk=74.25MHz,

Parameter		Symbol			Value			Unit	Note
					Min	Typ	Max		
Contrast Ratio		CR			104,000	130,000	-		1
Surface Luminance, white		L_{WH}	2D	Normal	104	130	-	cd/m²	2
				Peak	240	300	-		
				HDR 3%	320	400	-		
Luminance Uniformity		δ_{WHITE}	9P		75	80	-	%	3
Response Time	Gray-to-Gray	G to G			-	0.5	3	ms	4
	MPRT	MPRT				8	12	ms	5
Color Coordinates [CIE1931]	RED	Rx			Typ -0.02	0.678	Typ +0.02		
		Ry				0.321			
	GREEN	Gx				0.265			
		Gy				0.682			
	BLUE	Bx				0.142			
		By				0.050			
	WHITE	Wx				0.281			
		Wy				0.288			
Color Temperature						10,000		K	
Color Gamut	DCI CIE1976					98.5		%	
	sRGB					129		%	
Color Viewing Angle									
(Δu'v' ≤ 0.025)	x axis, right(ϕ=0°)	θr			60	-	-	degree	6
	x axis, left (ϕ=180°)	θl			60	-	-		
	y axis, up (ϕ=90°)	θu			60	-	-		
	y axis, down (ϕ=270°)	θd			60	-	-		
Life Time (B10)		Hrs			-	30,000	-		7, 10
Gray Scale					-	2.2	-		7, 9

Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.

2. Aging should be processed before measuring luminance. Aging means turning on the measurement pattern for 30minutes in a darkroom at 25±2°C. Luminance is measured at 50cm from center 1-point. Normal, Peak and HDR luminance are measured after Aging process, respectively. For more information, see the Fig. 2.
   ※ Measurement Pattern - Normal: APL 100% / Peak : APL 25% / HDR : APL 3%
3. The variation in surface luminance , δ WHITE is defined as :
   δ WHITE(9P) = Minimum($L_{on1,,}$…. L_{on9}) / Maximum(L_{on1}….. L_{on9})
   Where L_{on1} to L_{on9} are the luminance with all pixels displaying white at 9 locations .
   For more information, see the FIG. 2.
4. Response time is the time required for the display to transit from G(N) to G(M) (Rise Time, Tr_R) and from G(M) to G(N) (Decay Time, Tr_D). For additional information, see the FIG. 3. (N<M)
   ※ G to G Spec stands for average value of all measured points.
   Photo Detector : RD-80S / Field : 2°
5. MPRT is defined as the 10% to 90% blur-edge width Bij(pixels) and scroll speed U(pixels/frame)at the moving picture. For more information, see FIG 4.
6. Viewing Angle Color Shift (VACS) is defined as follows after measuring color coordinates at each angle.; VACS=sqrt(du2+dv2) (@ CIE (u', v') color space) For more information, see the FIG. 5.
7. Test Condition : IEC62087 standard video with OFF-RS every 4 hours at room temperature 25℃ (If the cumulative time of usage is over 4 hours, OFF-RS compensation should be performed.)
8. Gray scale specification.
   Gamma Value is approximately 2.2. For more information, see the Table 13.
9. Gamma measurement (For typical Value 2.2)
   1) Before Measurement, the AGING should be processed over30minutes in 3% sized box pattern with peak luminance and black background.
   2) After the AGING, measurement of Gamma curve should be checked by top-down order, 255 → 0 gray scale (i.e. 8 bit)
   ※ Result is changed by measurement pattern size between > 3% and ≤ 3%.
   (i.e Size of Aging pattern is equal to measurement pattern size.)
10. The life time is defined as the when brightness of OLED itself reach to the 50% of initial value under t the conditions at Ta = 25±2℃ and operating IEC62087 standard video data.

Table 13. Gray Scale Specification

Gray Level	Luminance [%] (Typ)
L0	0.001
L63	0.20
L127	0.97
L191	2.42
L255	4.61
L319	7.59
L383	11.4
L447	16.0
L511	21.6
L575	28.0
L639	35.4
L703	43.7
L767	53.0
L831	63.2
L895	74.5
L959	86.7
L1023	100

Measuring point for surface luminance & measuring point for luminance variation.

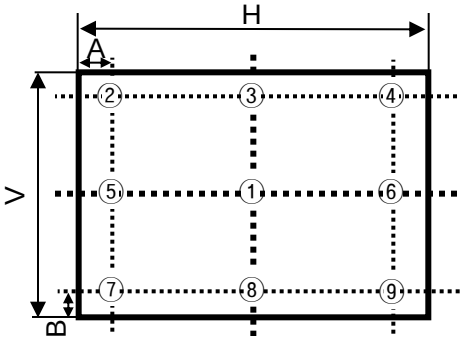


FIG. 2-1 9 Points for Luminance Measure with 100% APL

A: H/9 B: V/9 @ H,V: Active Area

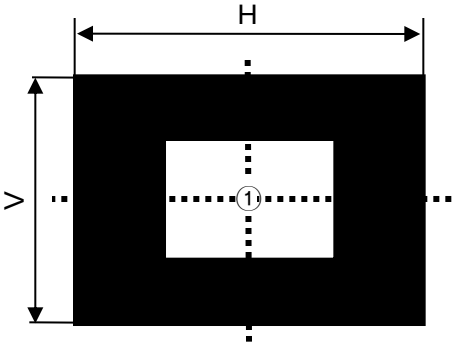


FIG. 2-2. 1 Point for peak luminance measure with 25% APL

@ H,V: Active Area

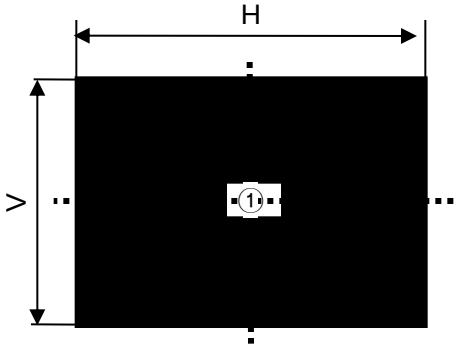
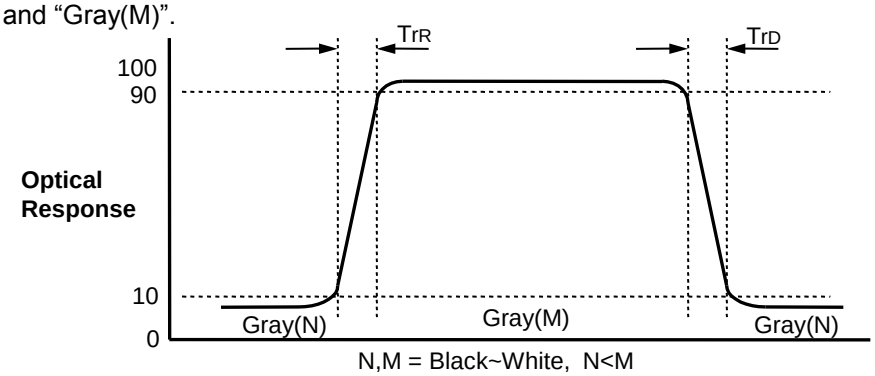


FIG. 2-3. 1 Point for HDR luminance measure with 3% APL

@ H,V: Active Area

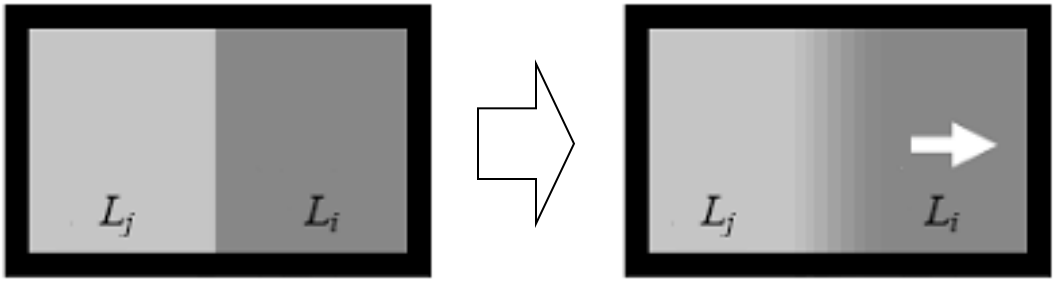
Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".



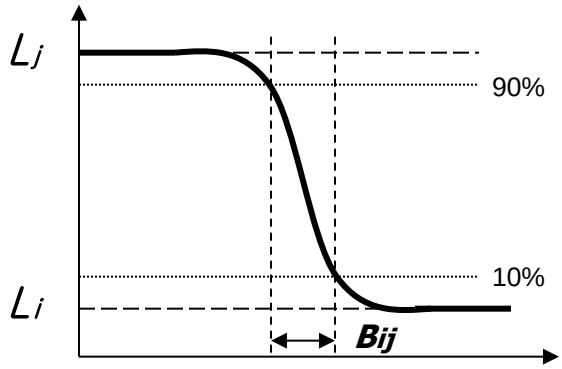
N,M = Black~White, N<M

FIG. 3 Response Time

MPRT is defined as the 10% to 90% blur-edge with Bij(pixels) and scroll speed U(pixels/frame)at the moving picture.



$$M = \frac{1}{U} Bij \ (i \neq j)$$



Example) Bij = 12pixels, U = 10pixels / 120Hz

M = 12pixels / (10pixels / 120Hz)

= 12pixels / {10pixels / (1/120)s}

= 12 / 1,200 s

= 10 ms

FIG. 4 MPRT

Dimension of viewing angle range

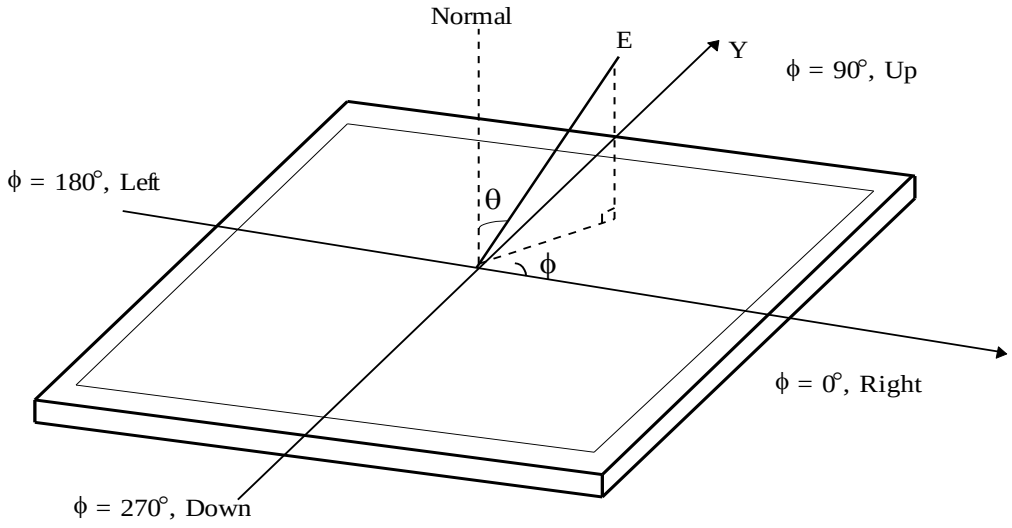


FIG. 5 Viewing Angle

5. Mechanical Characteristics

Table 14 provides general mechanical characteristics.

Table 14. Mechanical Characteristics

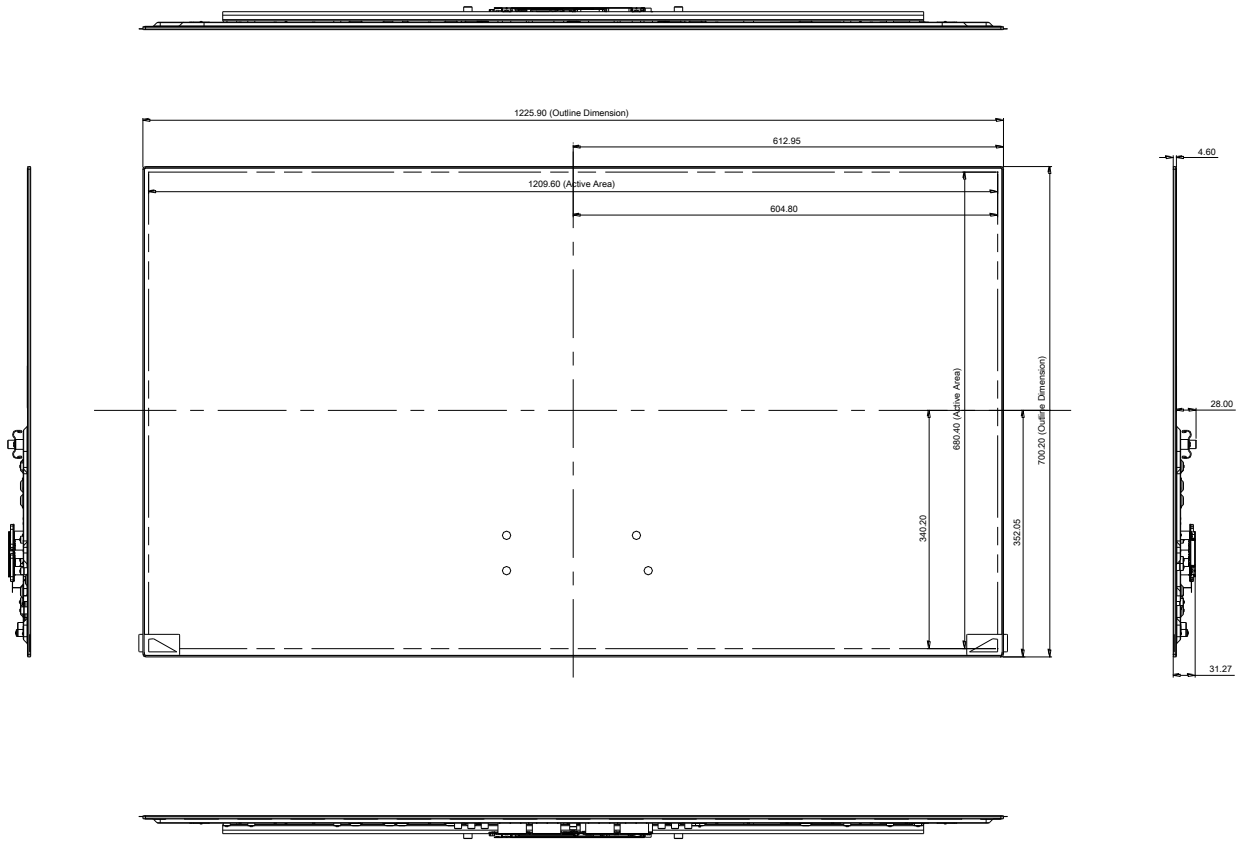
Item	Value	
Active Display Area (Base on Flat Panel)	Horizontal	1209.6mm
	Vertical	680.40mm
Weight	12.5 kg (Typ.), 13.8kg(Max)	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

Table 15. Mechanical Characteristics

Item	Value	
On Bezel **(Active Area ~ Edge of Module)**	Horizontal	8.15mm (Left) / 8.15mm (Right)
	Vertical	7.95mm (Top) / 11.85mm (Bottom)

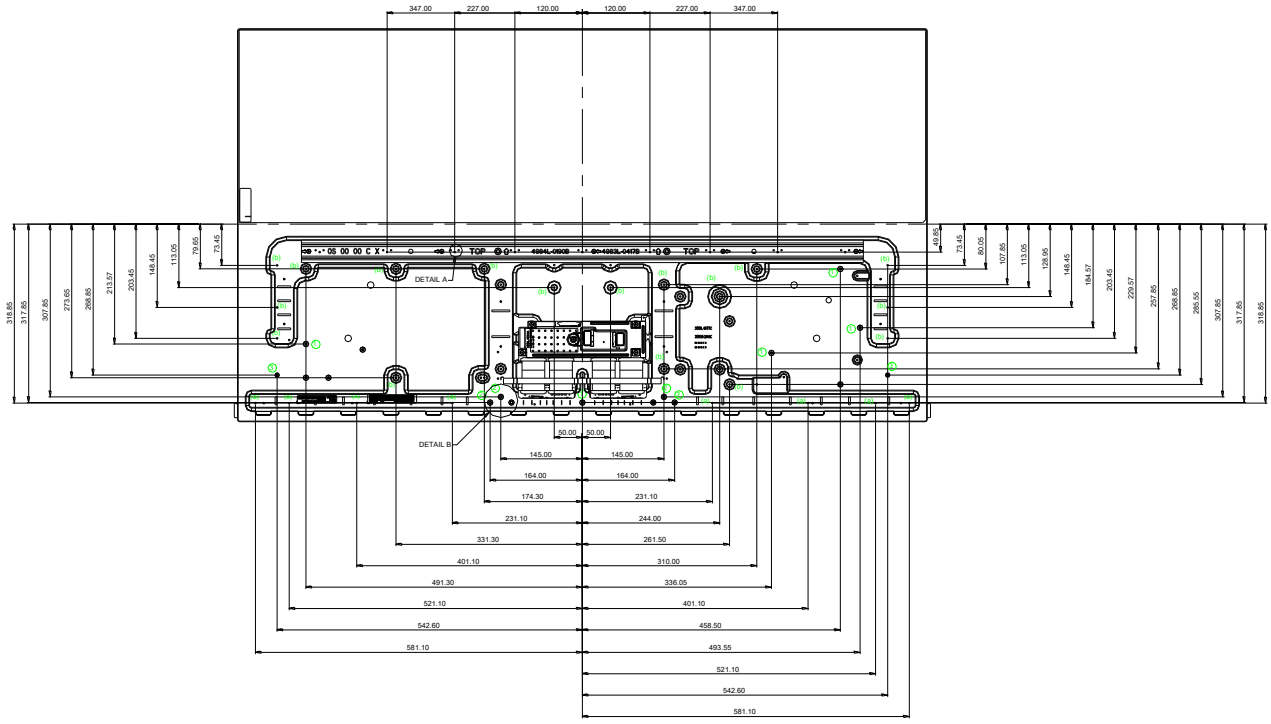
[FRONT VIEW]

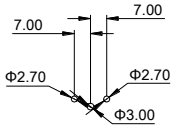


Date`	Version
18.09.13	0.1

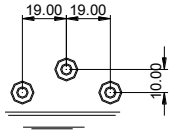
NOTE
1. Unspecified tolerance is ±1.0mm
2. Border Gap 0.0~1.2mm @ Power off, Room Temp.
3. The tapping type and depth for each mounting hole comply with the table " Pem-Nut information"

[REAR VIEW]

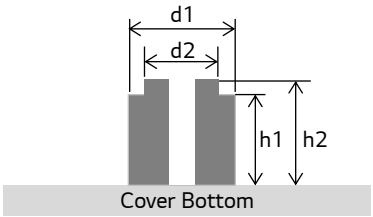




DETAIL A
SCALE 1/2



DETAIL B
SCALE 1/2



Item	Tap	Diameter		Height		Max Depth	Notes
		d1	d2	h1	h2		
①	M3	Φ10.0	Φ3.8	10.0	11.0	7.0	Second Stage Pem-Nut
②	M4	Φ10.0	-	8.0	-	5.5	
③	M3	Φ8.0	-	6.0	-	4.0	
④	M6	Φ12.0	-	9.8	-	12.0	
(a)	M3	-	-	-	-	3.0	Burring Tap
(b)	M3	-	-	-	-	5.0	Burring Tap
(c)	M3	-	-	-	-	2.0	Burring Tap

Date`	Version
18.09.13	0.1

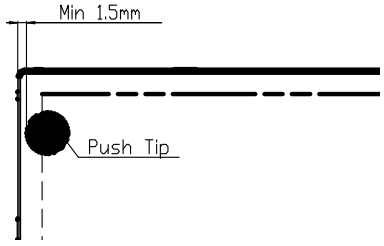
Note
1. Unspecified tolerance is ± 1.0mm
2. The tapping type and max. depth for each mounting hole comply with above table “Pem-nut information”
3. Border Gap : 0≤X≤1.2mm, (@Power off) Room Temperature.

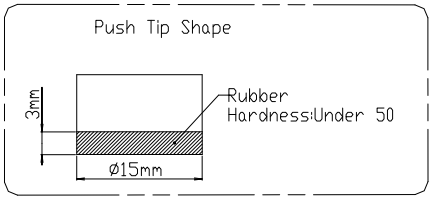
6. Reliability

Table 16. Environment Test Condition

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Pallet Packing Vibration test (non-operating)	Wave form : random Vibration level : 1.15Grms Bandwidth : 1-200Hz Duration : Z, 30 min
6	Humidity condition Operation	Ta= 40 °C ,90%RH
7	Altitude operating storage / shipment	0 - 15,000 ft 0 - 40,000 ft
8	Panel Push Test (Module Condition)	Max 6kgf (Note 2.)

Note : 1. Before and after Reliability test, OLED Module should be operated with normal function.
(After Reliability test, some OLED Module need to do OFF-RS before function check)
2. Panel Push Test Method. (The result should be no panel crack)





7. International Standards

7-1. Safety

(1) UL 60065, Seventh Edition, Underwriters Laboratories Inc.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

(2) CAN/CSA C22.2 No.60065:03, Canadian Standards Association.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

(3) EN 60065:2002 + A11:2008, European Committee for Electrotechnical Standardization (CENELEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

(4) IEC 60065:2005 + A1:2005, The International Electrotechnical Commission (IEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
(Including report of IEC60825-1:2001 clause 8 and clause 9)

7-2. Environment

(1) RoHS, Commission Delegated Directive (EU) 2015/863 of 31 March 2015 amending Annex II to Directive 2011/ 65 / EU of the European Parliament and of the Council

8. Packing

8-1. Information of OLED Module Label

(1) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M	N

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F : Date
G ~ N : SERIAL NO.

※ Date

Date	1 ~ 9	10 ~ 31
Mark	1 ~ 9	A ~ V

Note

1. YEAR

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Mark	A	B	C	D	E	F	G	H	J	K

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

(2) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the OLED module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one Pallet : 22 pcs

b) Pallet Size : 1440 mm(W) X 1140 mm(D) X 967 mm(H)

9. Precautions

Please pay attention to the followings when you use this OLED module.

9.1 Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(6) Please do not give any mechanical and/or acoustical impact to Module. Otherwise, Module can't be operated its full characteristics perfectly.
(7) A screw which is fastened up the steels should be a machine screw.
(if not, it can causes conductive particles and deal Module a fatal blow)
(8) Please do not set OLED on its edge.

9-2. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-3. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-4. Storage

When storing modules as spares for a long time, the following precautions are necessary.

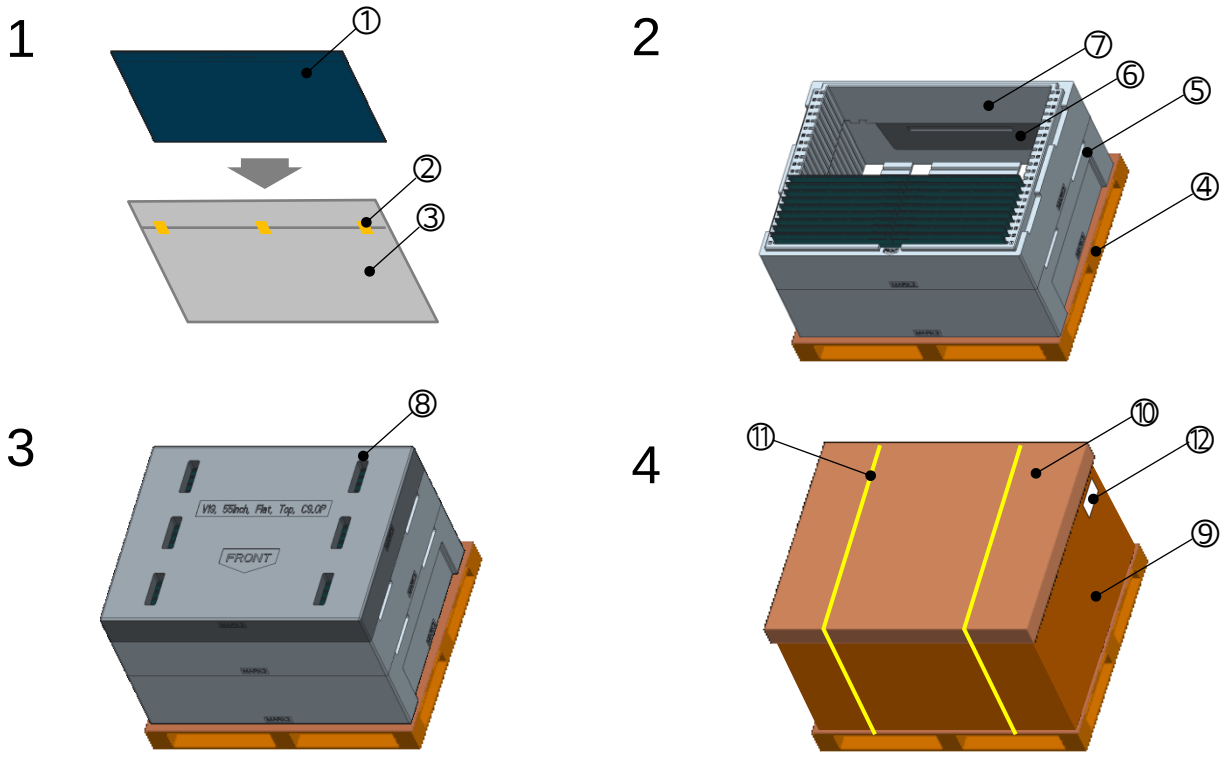
(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they are stored in the container in which they were shipped.

9-5. Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

APPENDIX - I

■ LW550AQD-EMA1 – Pallet Ass'y



※ Pallet Number of stackable stages: 3-stage loading

NO.	DESCRIPTION	MATERIAL
①	OLED Module	-
②	TAPE	Masking Tape
③	BAG	AL
④	PALLET	Plywood
⑤	PACKING, BOTTOM	EPS
⑥	PACKING, PAD	EPS
⑦	PACKING, MIDDLE	EPS
⑧	PACKING, TOP	EPS
⑨	ANGLE PACKING	Paper DW
⑩	ANGLE COVER	Paper SW
⑪	BAND	PP
⑫	LABEL	Yupo Paper

APPENDIX - II

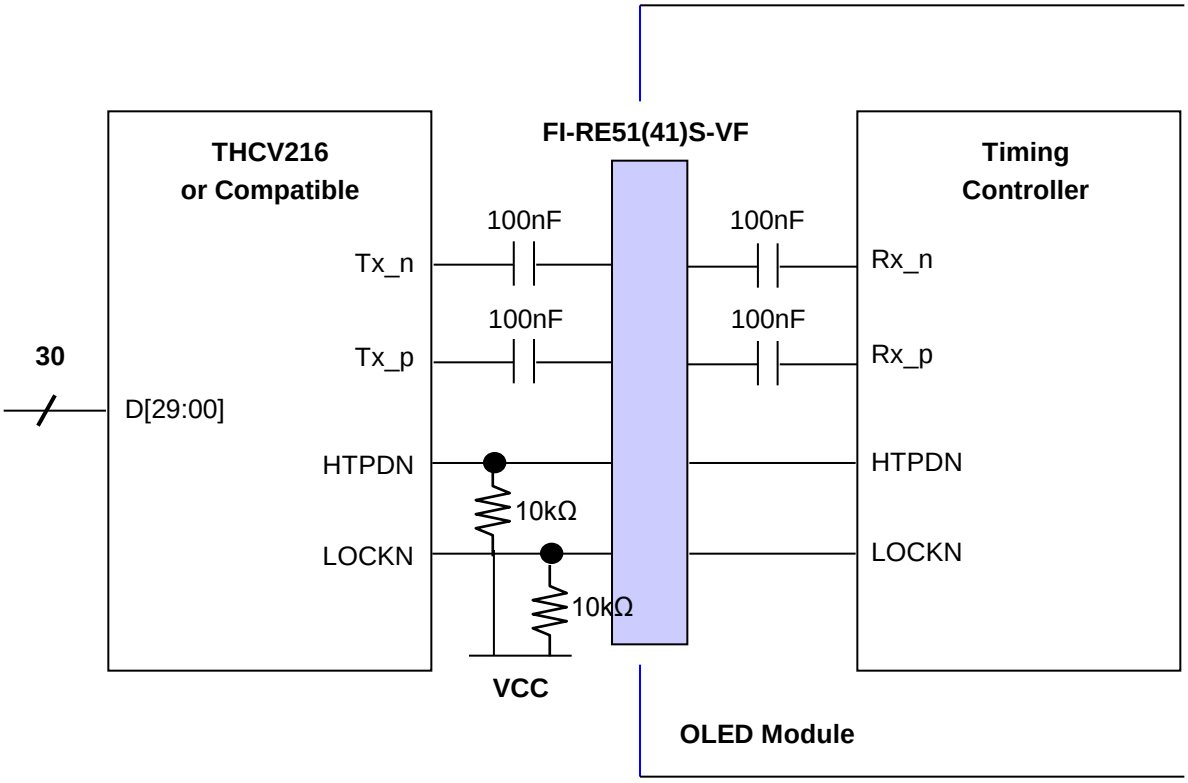
■ LW550AQD-EMA1-OLED Module Label

APPENDIX - III

■ Pallet Label

APPENDIX - IV

■ Required Signal Assignment for Flat Link (Thine : THCV215) Transmitter

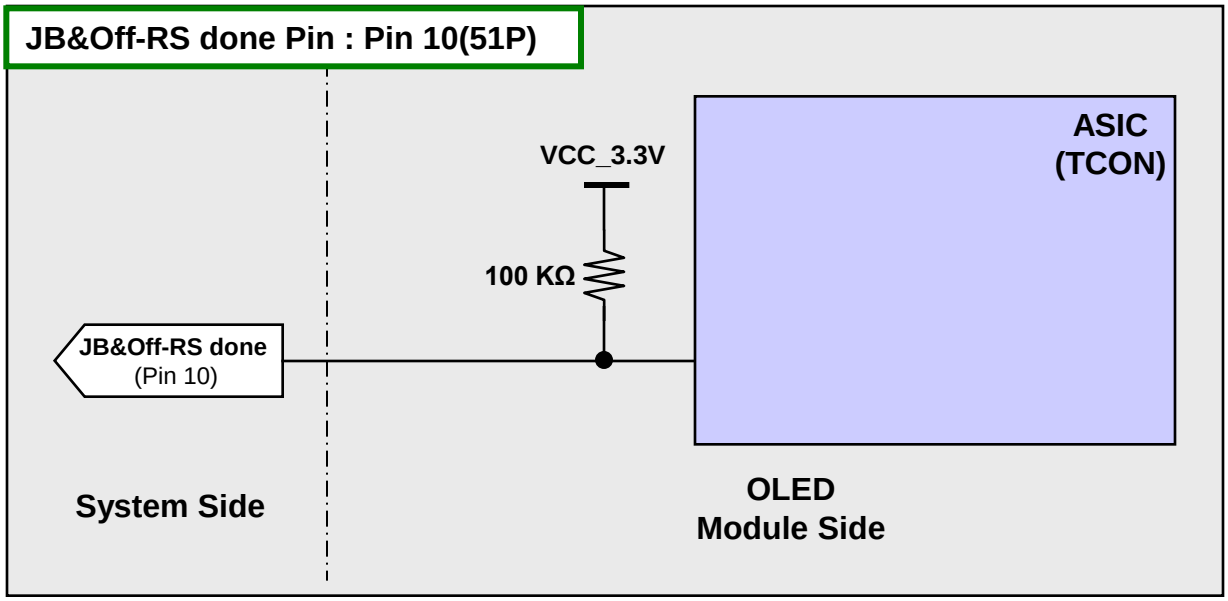


Note: 1. The OLED module uses a 100 nF capacitor on positive and negative lines of each receiver input.
2. Refer to VbyOne Transmitter Data Sheet for detail descriptions. (THCV216 or Compatible)
3. About Module connector pin configuration, Please refer to the Page 7~8.

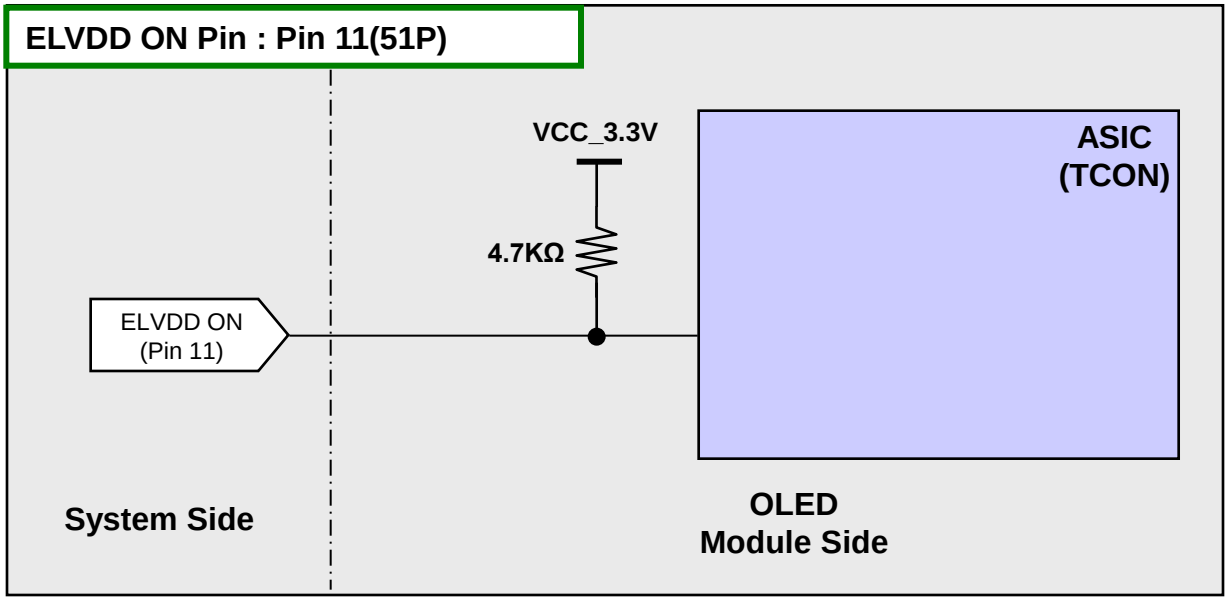
APPENDIX - V - 1

■ Circuit Block Diagram for Option Pin

(1) Circuit Block Diagram of **JB&Off-RS done** pin



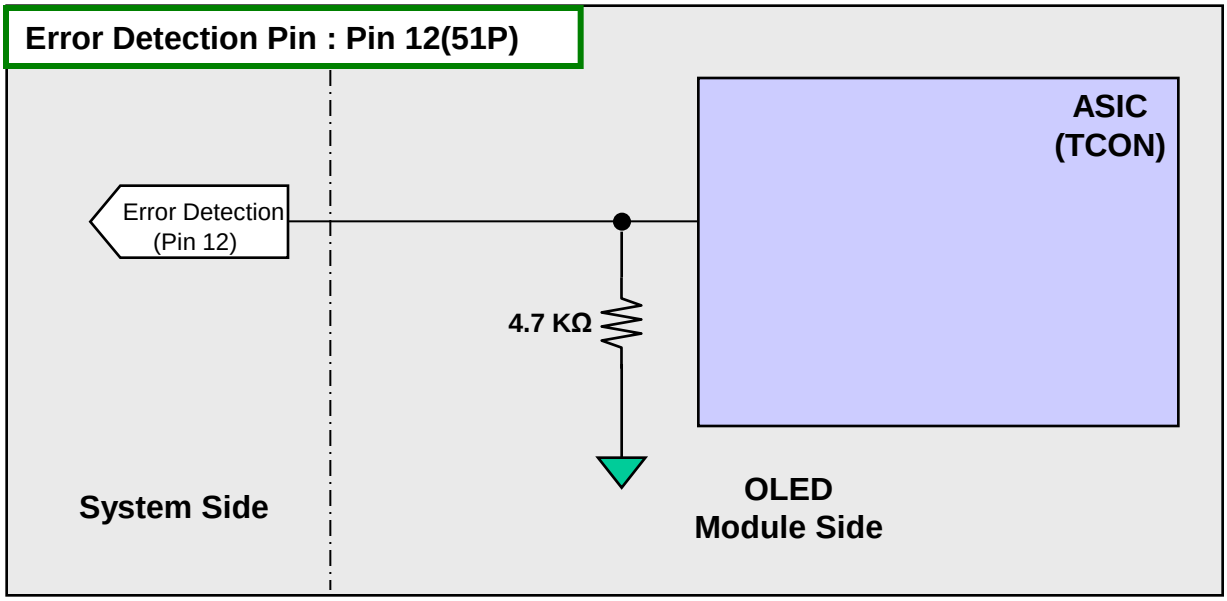
(2) Circuit Block Diagram of **AC_DET** pin



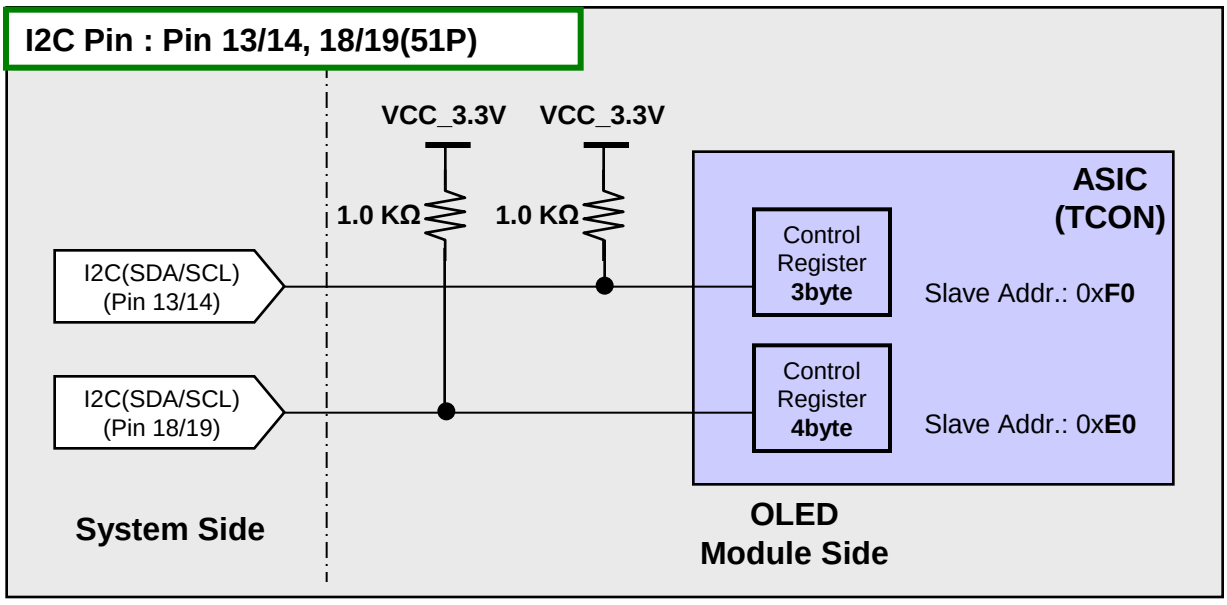
APPENDIX - V - 2

■ Circuit Block Diagram for Option Pin

(3) Circuit Block Diagram of **Error Detection** pin



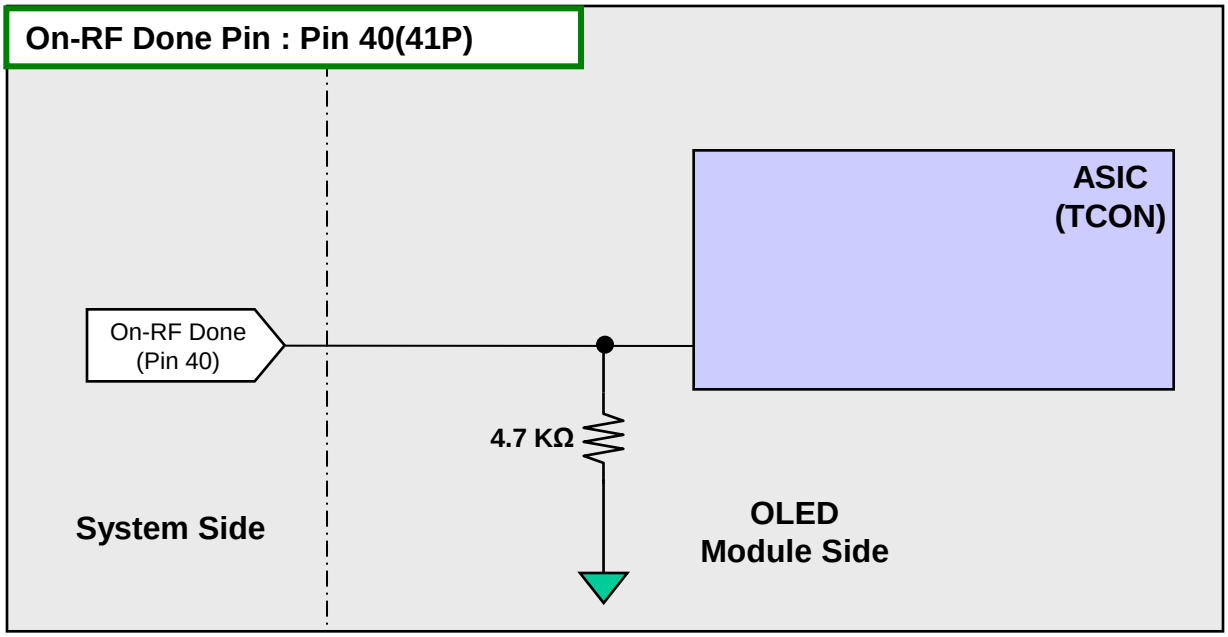
(4) Circuit Block Diagram of **I2C(SDA/SCL)** pin



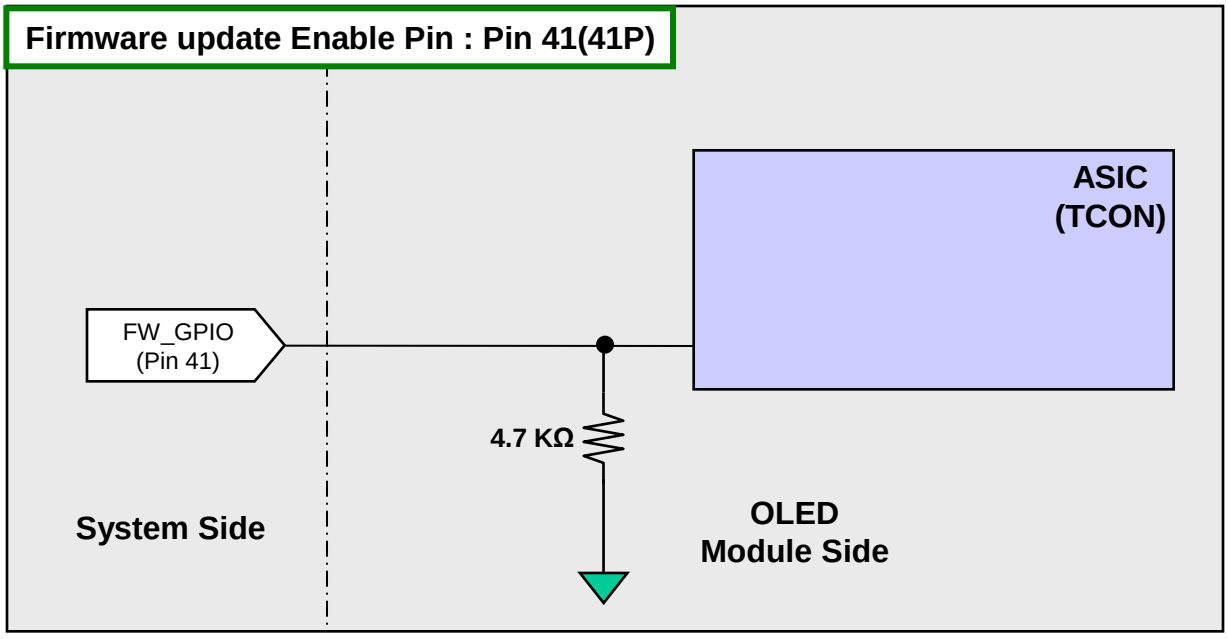
APPENDIX - V - 3

■ Circuit Block Diagram for Option Pin

(5) Circuit Block Diagram of **On-RF Done** pin



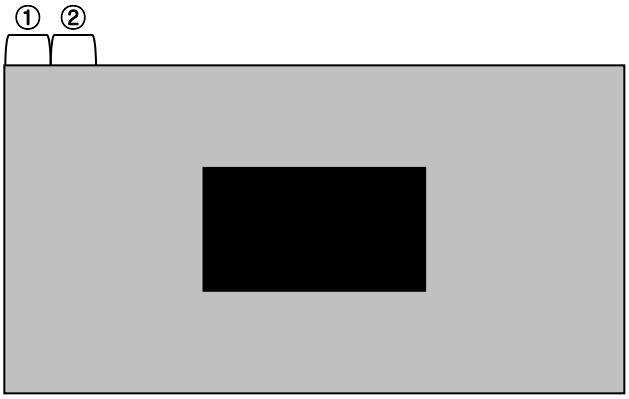
(6) Circuit Block Diagram of **FW_GPIO** pin



APPENDIX - VI - 2

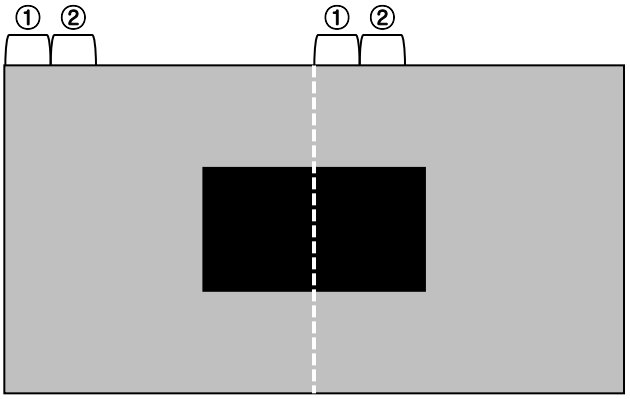
■ Input Mode of Pixel Data

Mode 1 : Non Division Mode



	1'st Data	2'nd Data	…	Data #
Lane00	1	17	…	3825
Lane01	2	18	…	3826
Lane02	3	19	…	3827
Lane03	4	20	…	3828
Lane04	5	21	…	3829
Lane05	6	22	…	3830
Lane06	7	23	…	3831
Lane07	8	24	…	3832
Lane08	9	25	…	3833
Lane09	10	26	…	3834
Lane10	11	27	…	3835
Lane11	12	28	…	3836
Lane12	13	29	…	3837
Lane13	14	30	…	3838
Lane14	15	31	…	3839
Lane15	16	32	…	3840

Mode 2 : 2 Division Mode

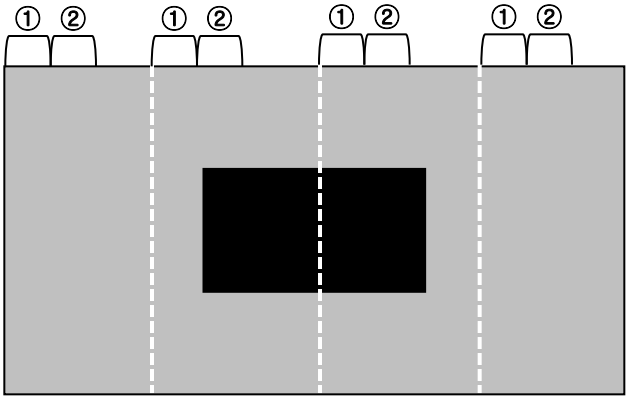


	1'st Data	2'nd Data	…	Data #
Lane00	1	9	…	1913
Lane01	2	10	…	1914
Lane02	3	11	…	1915
Lane03	4	12	…	1916
Lane04	5	13	…	1917
Lane05	6	14	…	1918
Lane06	7	15	…	1919
Lane07	8	16	…	1920
Lane08	1921	1929	…	3833
Lane09	1922	1930	…	3834
Lane10	1923	1931	…	3835
Lane11	1924	1932	…	3836
Lane12	1925	1933	…	3837
Lane13	1926	1934	…	3838
Lane14	1927	1935	…	3839
Lane15	1928	1936	…	3840

APPENDIX - VI

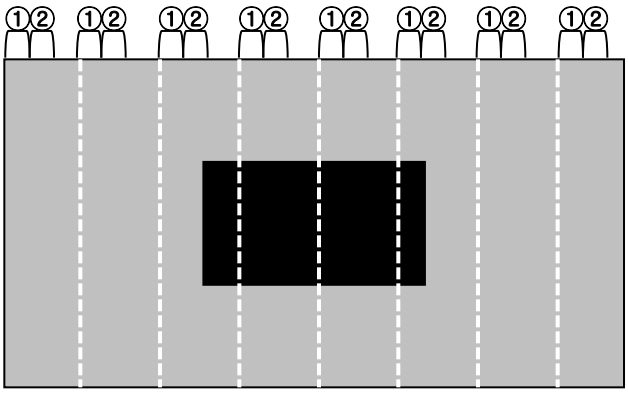
■ Input Mode of Pixel Data

Mode 3 : 4 Division Mode



	1'st Data	2'nd Data	…	Data #
Lane00	1	5	…	957
Lane01	2	6	…	958
Lane02	3	7	…	959
Lane03	4	8	…	960
Lane04	961	965	…	1917
Lane05	962	966	…	1918
Lane06	963	967	…	1919
Lane07	964	968	…	1920
Lane08	1921	1925	…	2877
Lane09	1922	1926	…	2878
Lane10	1923	1927	…	2879
Lane11	1924	1928	…	2880
Lane12	2881	2885	…	3837
Lane13	2882	2886	…	3838
Lane14	2883	2887	…	3839
Lane15	2884	2888	…	3840

Mode 4 : 8 Division Mode



	1'st Data	2'nd Data	…	Data #
Lane00	1	3	…	479
Lane01	2	4	…	480
Lane02	481	483	…	959
Lane03	482	484	…	960
Lane04	961	963	…	1439
Lane05	962	964	…	1440
Lane06	1441	1443	…	1919
Lane07	1442	1444	…	1920
Lane08	1921	1923	…	2399
Lane09	1922	1924	…	2400
Lane10	2401	2403	…	2879
Lane11	2402	2404	…	2880
Lane12	2881	2883	…	3359
Lane13	2882	2884	…	3360
Lane14	3361	3363	…	3839
Lane15	3362	3364	…	3840

APPENDIX - VII

■ Register Map

The following register is controlled by I2C Interface.

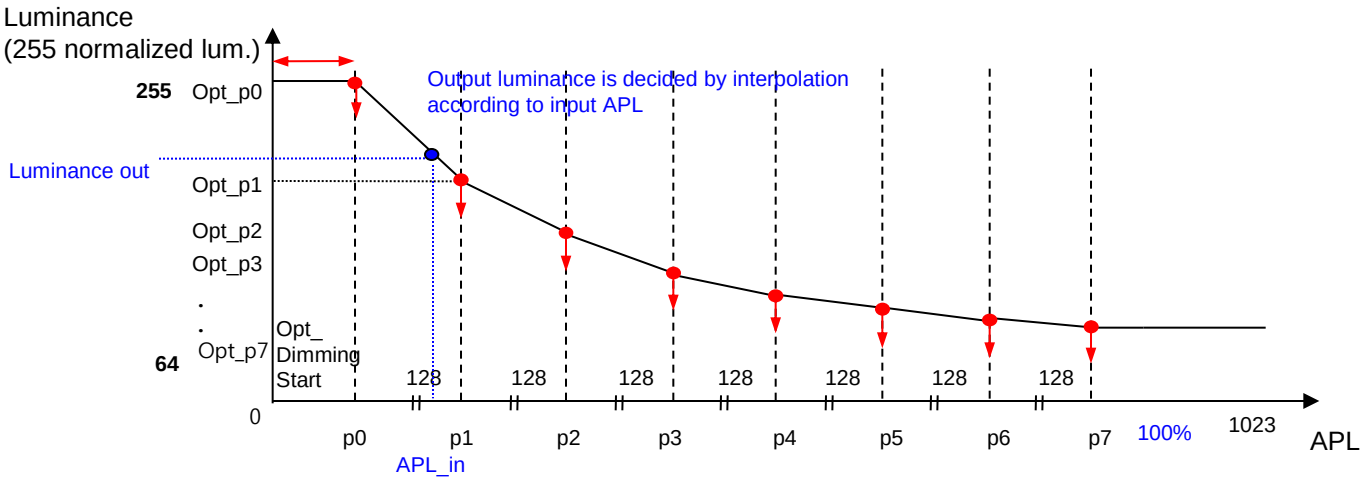
	Bit[7]: MSB	Bit[6]	Bit[5]					Bit[0]: LSB
Addr : 0x001	**CPC EN**	**TPC EN**	**RGB Max APL**	**OFF RS EN**	**APLC EM**	**WAPL EN**	**Opt_ Dimmin_ start[9]**	**Opt_ Dimming start[8]**

Device Address: 0xE0

Address [10:0]	Register Name	Description	Remark
0x000	Valid	Read only register (LGD use)	
0x001	[7] : CPC enable	1: enable, 0: disable	
	[6] : TPC enable	1: enable, 0: disable	
	[5] : RGB Max APL	1: RGB, 0: Y (BT.709)	
	[4] : Off RS enable	1: enable, 0: disable	
	[3] : APLC Enable	1: enable, 0: disable	
	[2] : WAPL enable	1: WAPL, 0 : normal APL	
	[1:0] Opt_Dimming_start[9:8]	APL value of P0 point	
0x002	Opt_Dimming_start[7:0]		
0x003	Opt_p0	APL P0 point corresponds to the 255 normalized luminance	(Opt_p0 /114) * 200 nit
0x004	Opt_p1	APL P1 point corresponds to the 255 normalized luminance	(Opt_p1 /114) * 200 nit
0x005	Opt_p2	APL P2 point corresponds to the 255 normalized luminance	(Opt_p2 /114) * 200 nit
0x006	Opt_p3	APL P3 point corresponds to the 255 normalized luminance	(Opt_p3 /114) * 200 nit
0x007	Opt_p4	APL P4 point corresponds to the 255 normalized luminance	(Opt_p4 /114) * 200 nit
0x008	Opt_p5	APL P5 point corresponds to the 255 normalized luminance	(Opt_p5 /114) * 200 nit
0x009	Opt_p6	APL P6 point corresponds to the 255 normalized luminance	(Opt_p6 /114) * 200 nit
0x00A	Opt_p7	APL P7 point corresponds to the 255 normalized luminance	(Opt_p7 /114) * 200 nit

Address [10:0]	Register Name	Description	Remark
0x00B	[7] LGE_PTN_FLAG	1: Pattern, 0: normal driving	
	[6:5] LEA mode sel.	b00: Normal operation, **b01 / b10 / b11: LGD reserved**	
	[4] LEA refresh en	1: LEA refresh , 0: Normal LEA	
	[3] : HDR_en	1: Enable, 0: Disable	
	[2] : Not used	LGD reserved	
	[1:0]:Opt WAPL_Dimming_start[9:8]	APL value of P0 point	Value Range: 0~1023
0x00C	Opt_WAPL_Dimming_start[7:0]		
0x00D	Opt_WAPL_p0	APL P0 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x00E	Opt_WAPL_p1	APL P1 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x00F	Opt_WAPL_p2	APL P2 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x010	Opt_WAPL_p3	APL P3 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x011	Opt_WAPL_p4	APL P4 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x012	Opt_WAPL_p5	APL P5 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x013	Opt_WAPL_p6	APL P6 point corresponds to the 255 normalized luminance	Value Range: 0~255
0x014	Opt_WAPL_p7	APL P7 point corresponds to the 255 normalized luminance	Value Range: 0~255

❑ PLC curve parameter

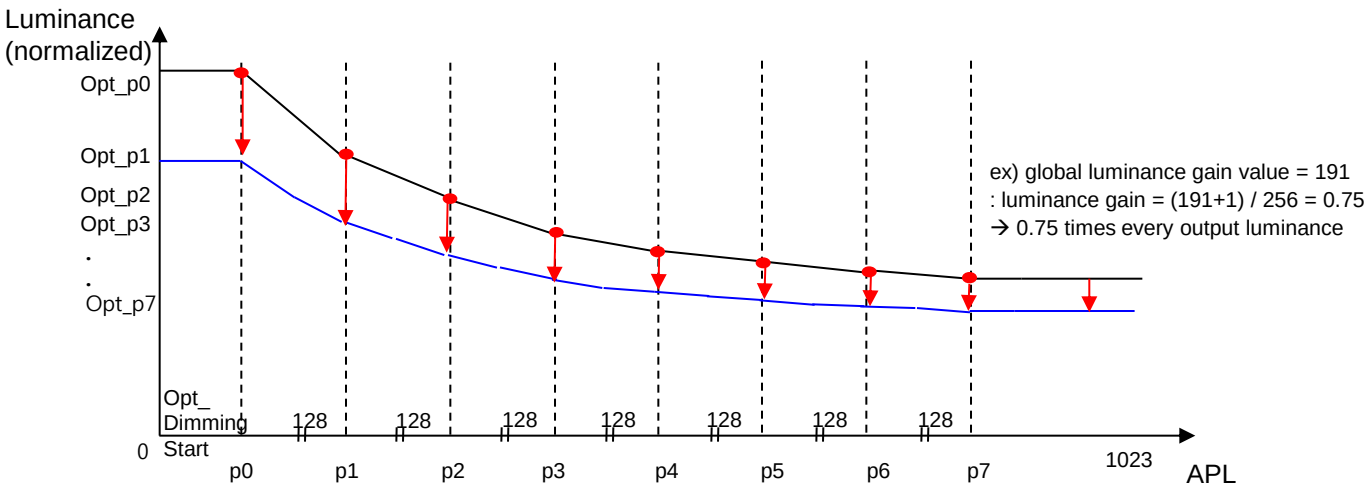


Every interval between each points except P0 is fixed to 128

- Luminance of p7~1023 interval are Opt_p7
- The point over 1023 is discarded

Address [10:0]	Register Name	Description	Remark
0x015	Opt_WAPL_luminance_gain	Adjust WAPL luminance gain	Value Range: 0~255
0x016	Opt_global_luminance_gain	Adjust global luminance gain 0~1 luminance gain according to 0~255 value (Same luminance gain is applied to every P0~P7 points)	Value Range: 0~255
0x017	Opt_ACL_PTN_ratio	Adjust ACL level gain for LGE PTN detect	Value Range: 0~255
0x05D	[7] vsJB_en	1: Enable, 0: Disable	
	[6:0] Not used	LGD reserved	
0x05E	Test_temp1[15:8]	1st temperature sensor	Read only
0x05F	Test_temp1[7:0]		
0x060	Test_temp2[15:8]	2nd temperature sensor	
0x061	Test_temp2[7:0]		

❑ Global luminance gain



Address [10:0]	Register Name	Description	Remark
0x07F	[7] : Not used	[7] Reserved	
	[6] : Not used	[6] Reserved	
	[5] : HDR EN@5byte mode only	1:11bit-HDR(HDR PASS mode) On, 0:10bit-HDR on	
	[4] : Reserved	[4] Reserved	
	[3:0] : The number of CTL data	The number of CTL data transmission channel for APL cross check(rage 3~16)	

APPENDIX - VIII - 1

■ Gray to Gray Response Time Uniformity

This is only the reference data of G to G and uniformity for LW550AQD-EMA1 model.

1. G to G Response Time :
   Response time is defined as FIG. 3 and shall be measured by switching the input signal for "Gray (N) " and "Gray(M)".(32Gray Step at 8bit)

2. G to G Uniformity
   The variation of G to G Uniformity , $\delta_{G\ to\ G}$ is defined as :

$$\text{G to G Uniformity} = \frac{Maximum(GtoG) - Typical(GtoG)}{Typical(GtoG)} \leq 1$$

*Maximum (GtoG) means maximum value of measured time (N, M = 0 (Black) ~ 1023(White), 128 gray step).

	0Gray	127ray	255Gray	…	895Gray	1023Gray
0Gray		TrR:0G→127G	TrR:0G→255G	…	TrR:0G→895G	TrR:0G→1023G
127Gray	TrD:127G→0G		TrR:127G→255G	…	TrR:127G→895G	TrR:127G→1023G
255Gray	TrD:255G→0G	TrD:255G→127G		…	TrR:255G→895G	TrR:255G→1023G
…	…	…	…		…	…
895Gray	TrD:895G→0G	TrD:895G→127G	TrD:895G→255G	…		TrR:895G→1023G
1023Gray	TrD:1023G→0G	TrD:1023G→127G	TrD:1023G→255G	…	TrD:1023G→895G	

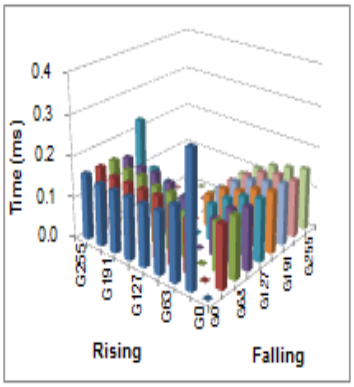
3. Sampling Size : 1 pcs

4. Measurement Method : Follow the same rule as optical characteristics measurement.

5. Current Status

   Below table is actual data of production on 12. 12. 2018 (LGD RV Event Sample)

	G to G Response Time [ms]		Average
	Min.	Max.	
# 1	0.06	0.32	0.14



Sample #1		Falling									Temperature
	Gray	G255	G223	G191	G159	G127	G95	G63	G31	G0	상온
Rising	G255	-	-	-	-	0.08	0.11	0.13	0.14	0.15	
	G223	-	-	-	-	0.08	0.11	0.13	0.14	0.14	Average (9 by
	G191	-	-	-	-	0.08	0.11	0.13	0.14	0.15	0.14
	G159	-	-	-	-	0.08	0.11	0.12	0.14	0.15	5 by 5
	G127	0.23	0.12	0.10	0.06	-	0.09	0.12	0.14	0.15	0.14
	G95	0.15	0.14	0.14	0.13	0.11	-	0.09	0.13	0.15	Standard Dev.
	G63	0.16	0.15	0.15	0.14	0.14	0.11	-	0.12	0.15	0.04
	G31	0.16	0.15	0.15	0.15	0.15	0.14	0.13	-	0.15	Max. / Min.
	G0	0.16	0.15	0.15	0.15	0.15	0.15	0.18	0.32	-	0.32 / 0.06

APPENDIX - VIII - 2

■ MPRT Response Time Uniformity(δ_{MPRT})

This is only the reference data of MPRT and uniformity for LW550AQD-EMA1 model.

(1) MPRT Response Time :
Response time is defined as FIG. 3.

(2) MPRT Uniformity
The variation of MPRT Uniformity , δ_{MPRT} is defined as :

$$\text{MPRT Uniformity} = \frac{Maximum\ (MPRT) - Typical\ (MPRT)}{Typical\ (MPRT)} \leq 1$$

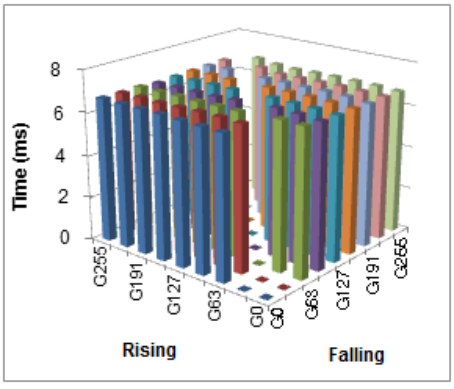
(3) Sampling Size : 2 pcs

(4) Measurement Method : Follow the same rule as optical characteristics measurement.

(5) Current Status

Below table is actual data of production on **12. 12. 2018 (LGD Event Sample)**

Sample	MPRT Response Time [ms]		Average
	Min.	Max.	
# 1	6.6	6.9	6.8
# 2	6.8	7.1	6.8

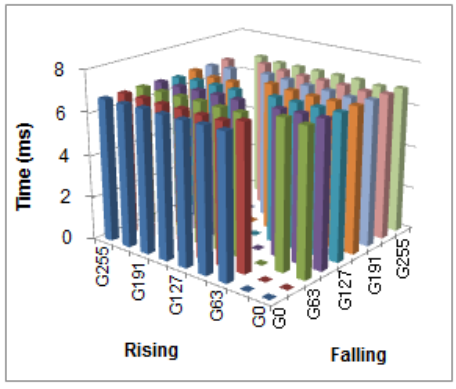


MPRT Rawdata

Max. Value
Min. Value

단위 : ms

Sample #1		Final Value									Temperature
	Gray	G255	G223	G191	G159	G127	G95	G63	G31	G0	상온
Initial Value	G255	-	6.9	6.8	6.8	6.8	6.8	6.8	6.8	6.7	
	G223	6.9	-	6.9	6.8	6.8	6.8	6.8	6.8	6.7	Average
	G191	6.8	6.8	-	6.8	6.8	6.8	6.8	6.8	6.7	6.8
	G159	6.8	6.8	6.8	-	6.8	6.8	6.8	6.8	6.7	Standard Dev.
	G127	6.7	6.8	6.8	6.8	-	6.8	6.8	6.8	6.7	0.1
	G95	6.7	6.7	6.7	6.7	6.8	-	6.9	6.8	6.7	Maximum
	G63	6.8	6.8	6.8	6.7	6.8	6.8	-	6.9	6.8	6.9
	G31	6.7	6.8	6.7	6.7	6.8	6.8	6.7	-	-	Minimum
	G0	6.7	6.7	6.7	6.7	6.7	6.7	6.6	-	-	6.6



단위 : ms

Sample #2		Final Value									Temperature
	Gray	G255	G223	G191	G159	G127	G95	G63	G31	G0	상온
Initial Value	G255	-	7.0	6.9	6.9	6.9	6.9	6.9	6.8	6.9	
	G223	6.9	-	7.1	6.9	6.9	6.9	6.8	6.8	6.9	Average
	G191	6.8	6.9	-	7.0	6.9	6.9	6.8	6.8	6.9	6.8
	G159	6.8	6.7	6.7	-	7.0	6.9	6.8	6.8	6.9	Standard Dev.
	G127	6.7	6.8	6.8	6.8	-	6.8	6.8	6.8	6.8	0.1
	G95	6.7	6.7	6.8	6.8	6.8	-	6.8	6.8	6.9	Maximum
	G63	6.7	6.7	6.7	6.7	6.7	6.7	-	7.0	6.9	7.1
	G31	6.7	6.7	6.7	6.7	6.6	6.6	6.8	-	-	Minimum
	G0	6.7	6.7	6.7	6.7	6.7	6.7	6.7	-	-	6.6